

# Model : Calpella

## Intel Calpella CPU + Intel PCH Chipset


PCB1  
PCB  
37GC42200-C0

C42IIX Main BD REV.C  
P/N: 37GC42200-C0  
Made in China

Calpella			
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10	DDR3 SO-DIMM Channel A,B		
11	Ibex Peak_RTC & SATA_a		
12	Ibex Peak_PCIE & MMB_b		
13	Ibex Peak_LVDS & DMI_c		
14	Ibex Peak_PCI & USB_d		
15	Ibex Peak_GPIO_f		
16	Ibex Peak_Power1_g		
17	Ibex Peak_Power2_h		
18	Ibex Peak_M_GND		
19	CLOCK GEN (ICS9LRS3197)		
20	LCD		
21	CRT/TPM/G-SENSOR		
22	MINI CARD/ODD/HDD/MDC CON		
23	CCD/BT/USB CON/3G & LED		
24	LAN - RTL8111DL-GR		
25	DVI SHIFTER/HDMI		
26	Audio Codec ALC269		
27	EC-IT8502NX/BIOS/FAN		
28	POWER SWITCH		
29	DC IN & CHARGER (OZ8618)		
30	+CPU_CORE (OZ8291)		
31	+GFX_CORE (OZ8291)		
32	0.75_DDR/1.8VS/1.1VS		
33	+1.1VS_VTT (OZ8111)		
34	+1.5 (OZ8116)		
35			
36			

AOI	ICT	ATS	CHR	I/D	F/T	PCBA	T/Q

Revision History		
	8/2009	Initial RA
	10/2009	RB
	12/2009	RC



ECS COMPUTER CORP.

Title

COVER PAGE

Size

Document Number

Rev

B

SCHEMATIC1

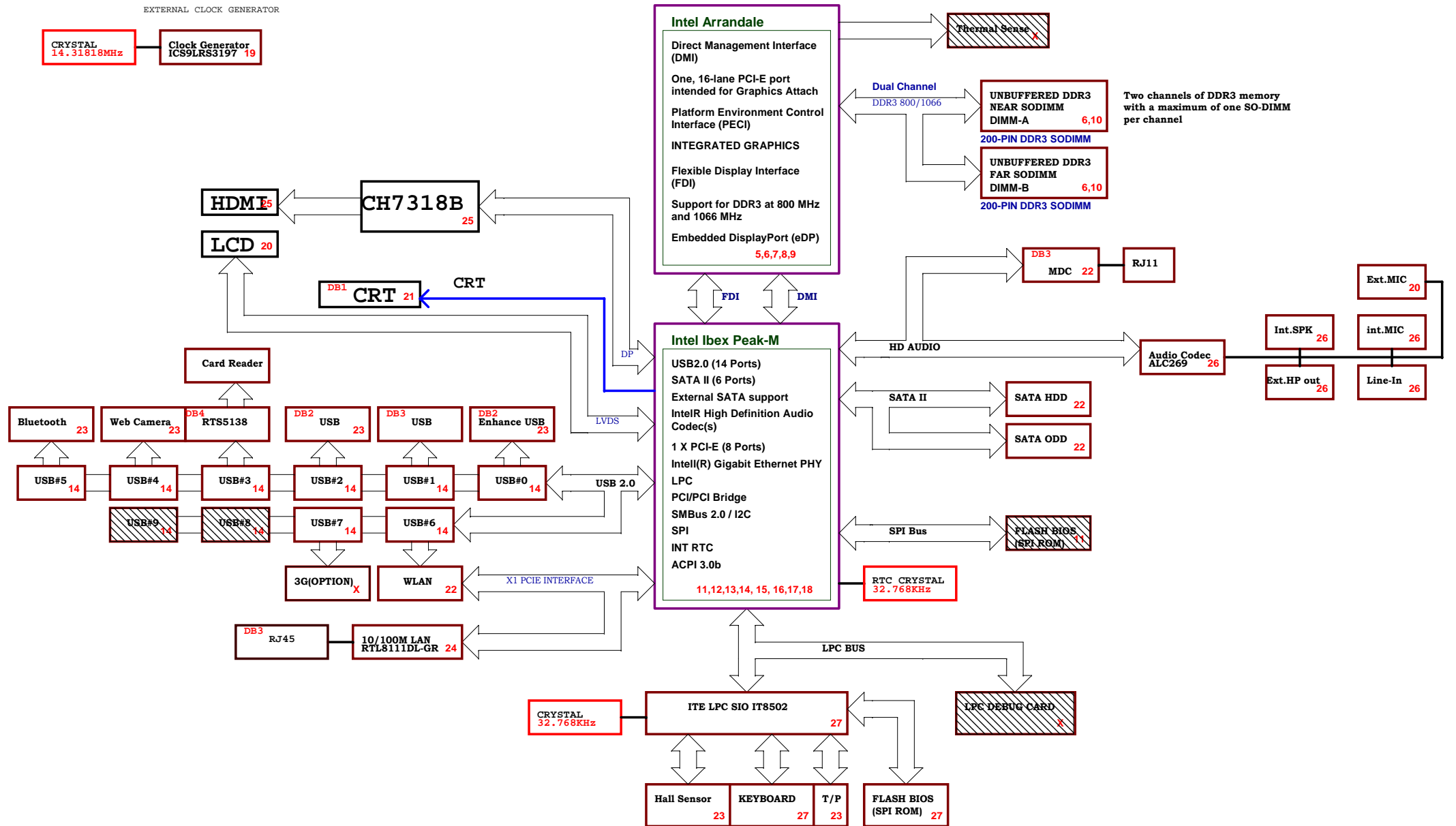
C

C42IIX

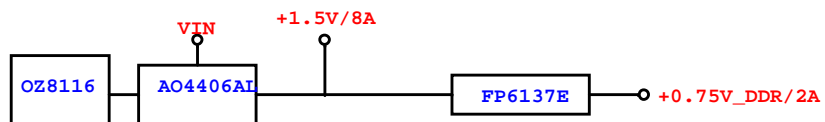
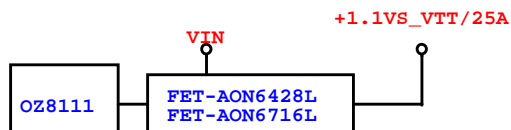
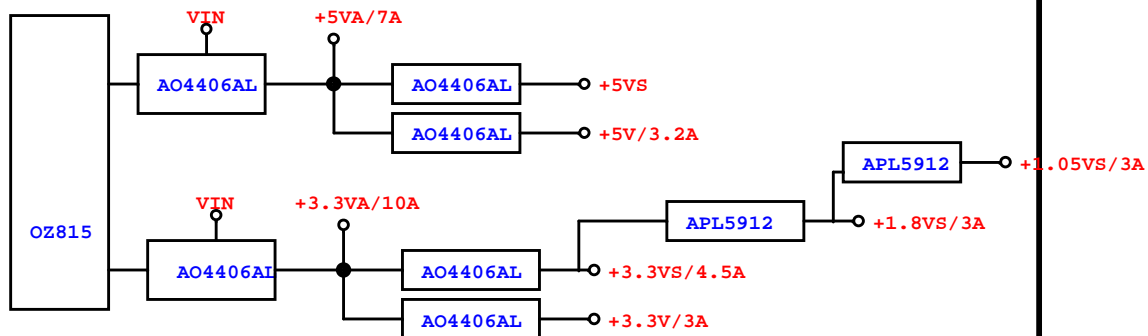
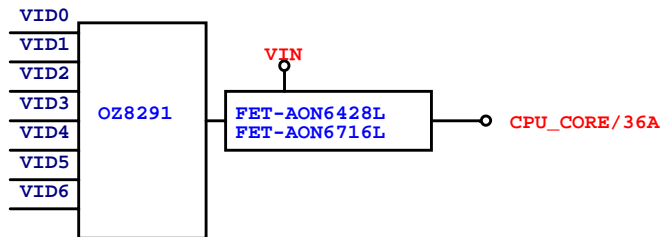
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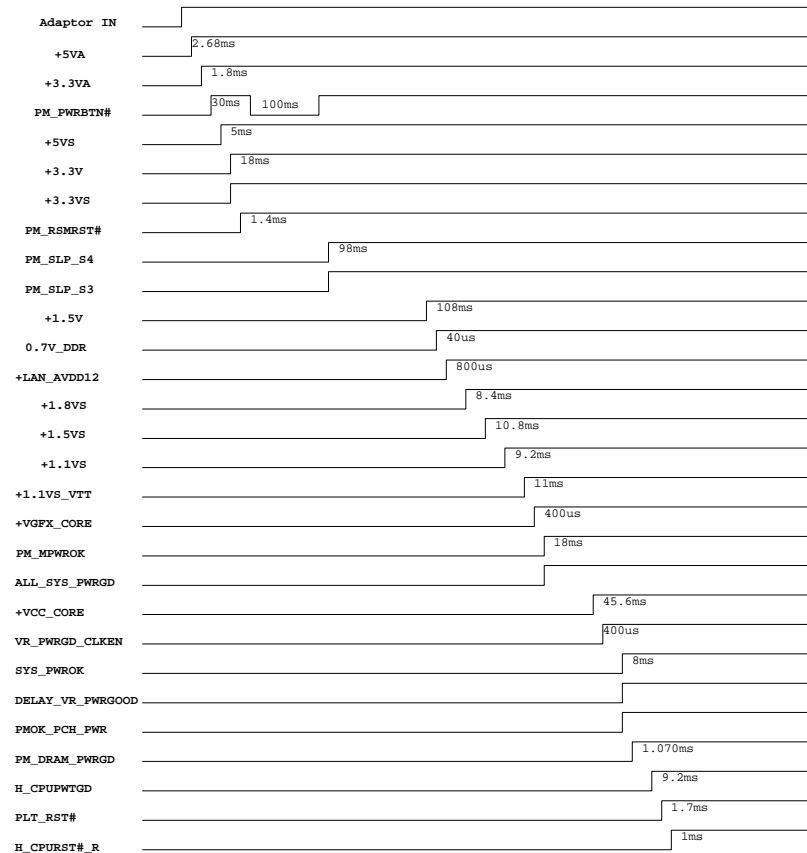
# C42IIX Calpella SYSTEM BLOCK DIAGRAM



# POWER BLOCK DIAGRAM



## Power up sequence



PCH GPIO	
GPIO0	S_GPIO
GPIO1	SMC_RUNTIME_SCI#
GPIO2	INT_PIRQ#
GPIO3	INT_PIRQ#
GPIO4	INT_PIRQ#
GPIO5	INT_PIRQ#
GPIO6	DGPU_HPD_INTR#
GPIO7	NC
GPIO8	HOST_ALERT#2
GPIO9	USB_OC#_10_11
GPIO10	USB_OC#_12_13
GPIO12	GPIO12
GPIO13	NC
GPIO14	USB_OC#_13_14
GPIO15	HOST_ALERT#1
GPIO16	DGPU_HOLD_RST#
GPIO17	DGPU_PWROK
GPIO18	CLK_MINI1_OE#
GPIO19	SATA_DET1#
GPIO20	CLK_PCIE_LAN_REQ#
GPIO21	SATA_DET0#
GPIO22	BIOS_REC
GPIO23	NC
GPIO24	NC
GPIO25	NC
GPIO26	NC
GPIO27	NC
GPIO28	SPI_CS#2
GPIO29	USB_OC#5
GPIO30	SUB_PWR_ACK
GPIO31	AC_PRESENT
GPIO32	PM_CLKRUN#
GPIO33	HDADOCKEN#_R
GPIO34	NC
GPIO35	NC
GPIO36	DGPU_PWR_EN#
GPIO37	DGPU_PRSENT#
GPIO38	MFG_MODE
GPIO39	CRB_SV_DET
GPIO40	USB_OC#_2_3
GPIO41	USB_OC#_4_5
GPIO42	USB_OC#_6_7
GPIO43	USB_OC#_8_9
GPIO50	PCI_REQ#1
GPIO51	PCI_GNT#1
GPIO52	DGPU_SELECT#
GPIO53	NC
GPIO54	PCI_REQ#3
GPIO55	PCI_GNT#3
GPIO44	NC
GPIO45	NC
GPIO46	RST_GATE
GPIO48	SV_SET_UP
GPIO49	CRIT_TEMP_REP#_R
GPIO56	NC
GPIO57	PCH_GPIO57
GPIO58	SMB1_CLK_EC
GPIO59	USB_OC#_0_1
GPIO61	PM_SUS_STAT#
GPIO72	PM_BATTLOW#
GPIO74	LPD_SPI_INTR#
GPIO75	SMB1_DAT_EC

ITE8502NX GPIO Pin Definition list	
GPA0	BTL_BEEP
GPA1	EC_BL_PWM
GPA2	LS_OFF#
GPA3	CCD_EN
GPA4	RF_LED_EC#
GPA5	Mini_Card_PWR_ON#
GPA6	MINI_RFON
GPA7	BT_ON
GPB0	SENBAT_V
GPB1	ALL_SYS_PWRGD
GPB2	+1.1VS_ON
GPB3	BAT_SMBCLK
GPB4	BAT_SMBDAT
GPB5	H_A20GATE
GPB6	H_RCIN#
GPB7	VCORE_ON
GPC0	+1.8VS_ON
GPC1	SMB_CLK_EC_CLK
GPC2	SMB_DATA_EC_CLK
GPC3	SAFETY
GPC4	+3.3VS_ON
GPC5	+5VS_ON
GPC6	+1.1VS_VTT_ON
GPC7	PM_PWRBTN#
GPD0	AC_IN
GPD1	INT1
GPD2	PLT_RST#
GPD3	ECSCI#
GPD4	
GPD5	AC_PRESENT
GPD6	+1.5V_ON
GPD7	+1.5VS_ON
GPE0	PM_RSMRST#
GPE1	VGA_CORE_ON
GPE2	PM_MPWROK
GPE3	+1.8VS_ON_ATI
GPE4	PWRON
GPE5	VDDR3_ON
GPE6	Low Voltage
GPE7	MUTE_AMP#
GPF0	EC_PROCHOT
GPF1	CHG_R_LED
GPF2	CHG_B_LED
GPF3	PWR_LED
GPF4	TP_CLK
GPF5	TP_DATA
GPF6	SMB_CLK_G
GPF7	SMB_DATA_G
GPH0	PWR_KEEP
GPH1	GPIO33
GPH2	
GPH3	PCH_SPI_CS
GPH4	PCH_SPI_CLK
GPH5	PCH_SPI_SO
GPH6	PCH_SPI_SI
GPG1	+3.3V_ON
ADC0/GPI0	BATT_TEMP
ADC1/GPI1	ADAPTOR_I
ADC2/GPI2	BAT_I
ADC3/GPI3	BAT_V
ADC4/GPI4	RF_SW
ADC5/GPI5	PM_SLP_S4#
ADC6/GPI6	PM_SLP_S3#
ADC7/GPI7	SUB_PWR_ACK

ITE8502NX GPIO	
DAC0/GPJ0	Fast-charge-EN
DAC0/GPJ1	CHG_I
DAC0/GPJ2	FAN_CTRL1
DAC0/GPJ3	CHG_ON
DAC0/GPJ4	USB0_EN#
DAC0/GPJ5	SET_V

ITE8502NX KB Matrlk interface	
KS10/STB#	KB_SIN0
KS11/AFD#	KB_SIN1
KS12/INIT#	KB_SIN2
KS13SLIN#	KB_SIN3
KS14	KB_SIN4
KS15	KB_SIN5
KS16	KB_SIN6
KS17	KB_SIN7
KS00/PD0	KB_SOUT0
KS01/PD1	KB_SOUT1
KS02/PD2	KB_SOUT2
KS03/PD3	KB_SOUT3
KS04/PD4	KB_SOUT4
KS05/PD5	KB_SOUT5
KS06/PD6	KB_SOUT6
KS07/PD7	KB_SOUT7
KS08/ACK#	KB_SOUT8
KS09/BUSY	KB_SOUT9
KS010/PE	KB_SOUT10
KS011/ERR#	KB_SOUT11
KS012/SLCT	KB_SOUT12
KS013	KB_SOUT13
KS014	KB_SOUT14
KS015	KB_SOUT15

ITE8502NX SPI Flash ROM interface	
FLFRAME#/GPG2	FLFRAME#
FLAD0/SCE#	EC_SPI_CS#
FLAD1/S1	EC_SPI_SI
FLAD2/S2	EC_SPI_SO
FLAD3/GPG6	LID#
FLCLK/SCK	EC_SPI_CLK
FLRST#/WU17 /GPG0 /TW	LCDSW

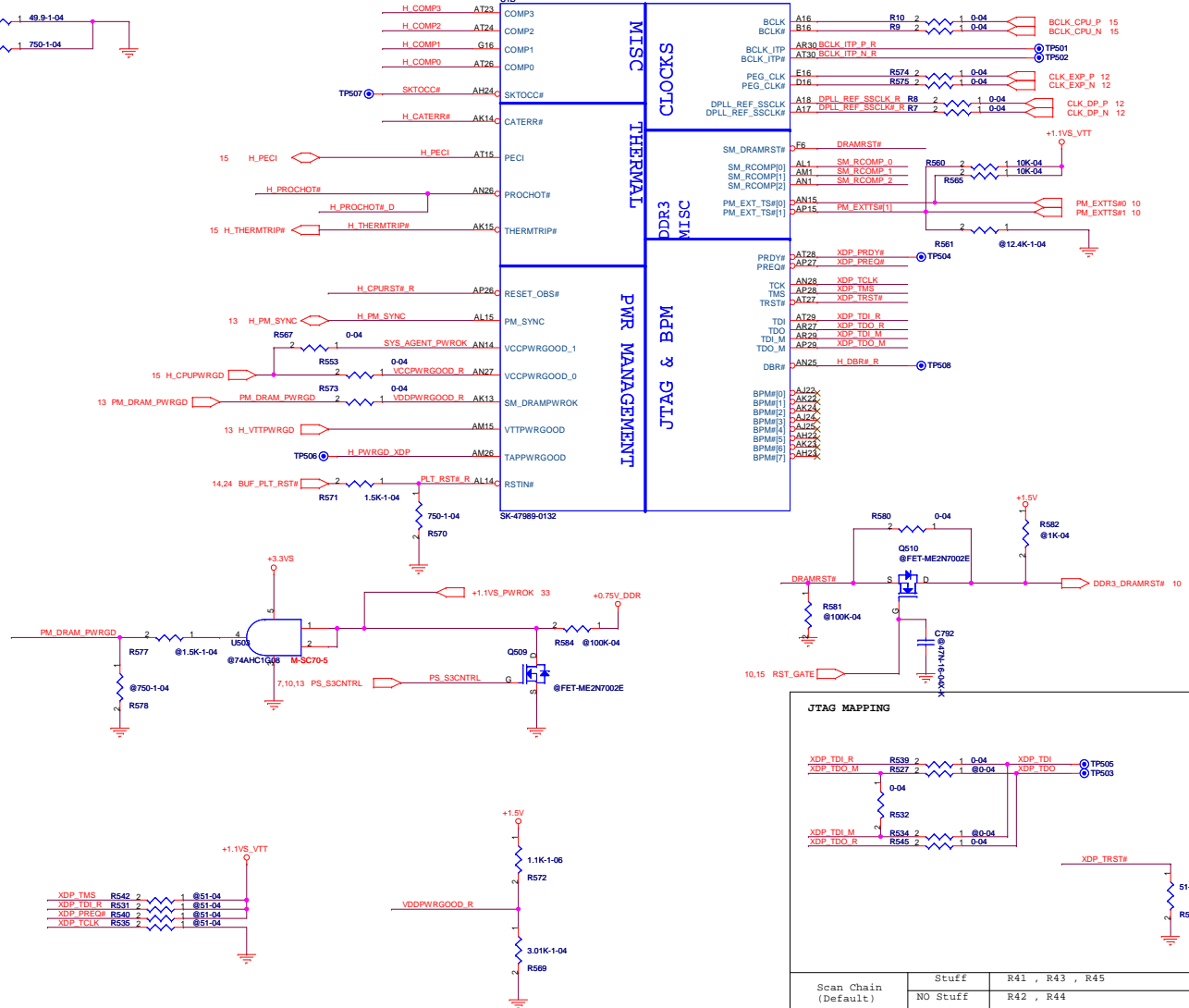
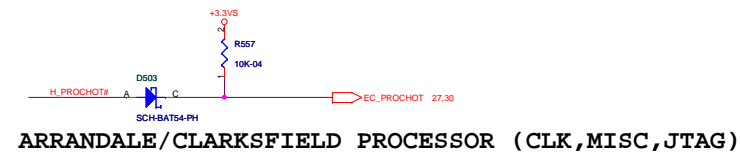
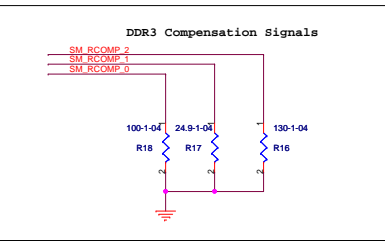
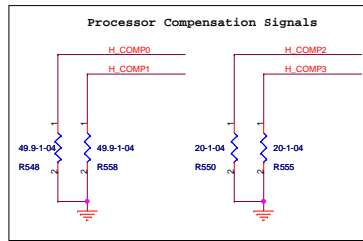
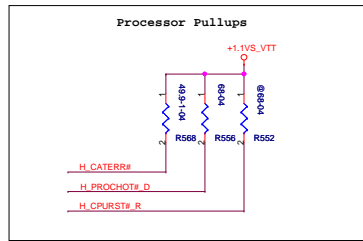
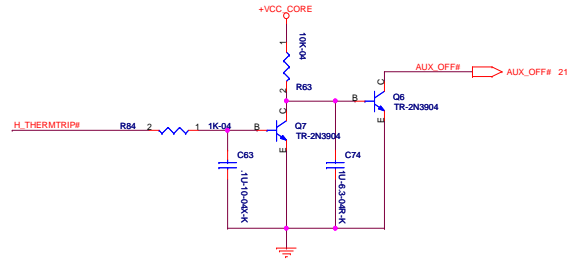
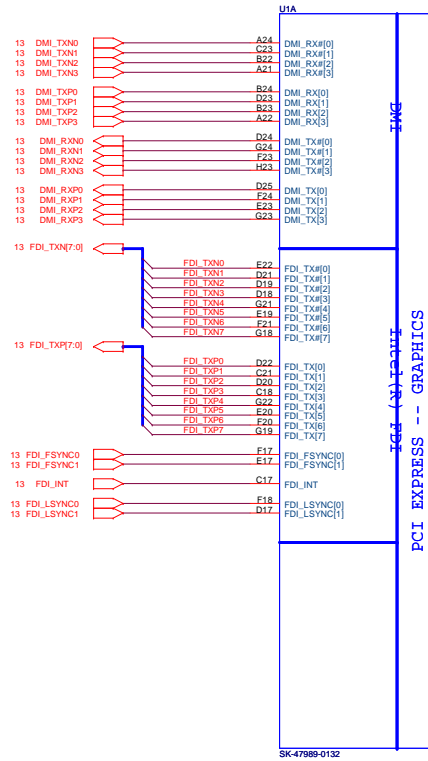
ITE8502NX System & LPC Bus	
LAD0	LPC_AD0
LAD1	LPC_AD1
LAD2	LPC_AD2
LAD3	LPC_AD3
SERIRQ	INT_SERIRQ
LFRAME#	LPC_FRAME#
LPCLK	CLK_PCI_KBC
WRST#	LRST1#

ITE8502NX Clock	
CLK32K	EC32KI
CK32KE	EC32KO

ITE8502NX Power	
VSTBY0	+3.3VA
VSTBY1	+3.3VA
VSTBY2	+3.3VA
VSTBY3	+3.3VA
VSTBY4	+3.3VA
VSTBY5	+3.3VA
VBAT	+3.3VA_RTC
AVCC	+3.3VA
VCC	+3.3VS

ITE8502NX GND	
AVSS	GND
VSS0	GND
VSS1	GND
VSS2	GND
VSS3	GND
VSS4	GND
VSS5	GND
VSS6	GND

## AUBURNDALE/CLARKSFIELD PROCESSOR(DMI,PEG,FDI)



**JTAG MAPPING**

The diagram illustrates the JTAG mapping for the R532 processor. The JTAG pins (XDP\_TDI\_R, XDP\_TDO\_M, XDP\_TDI\_M, XDP\_TDO\_R) are connected to the R532 processor pins (R539, R527, R534, R545) through a network of resistors (R532, R533, R534, R545) and logic inverters (0-04, @0-04). The JTAG pins are also connected to the TP505 and TP503 test points. The XDP\_TRST# pin is connected to the R544 pin through a resistor (R544) and a logic inverter (0-04).

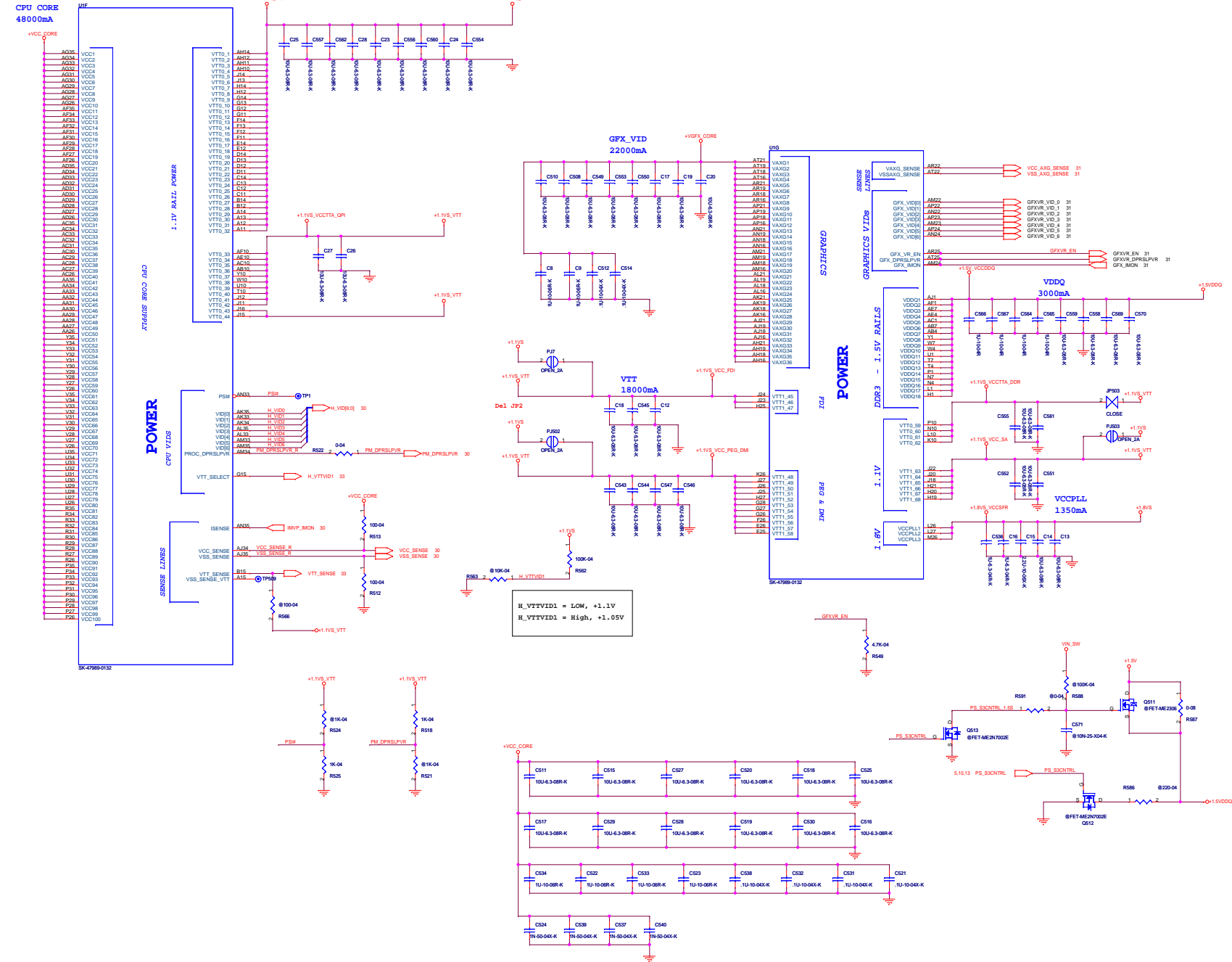
Scan Chain (Default)	Stuff	R41, R43, R45
	NO Stuff	R42, R44
	Stuff	R41, R42
CPU Only	NO Stuff	R43, R44, R45
	Stuff	R44, R45
GMCH Only	NO Stuff	R41, R42, R43



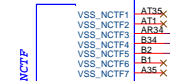
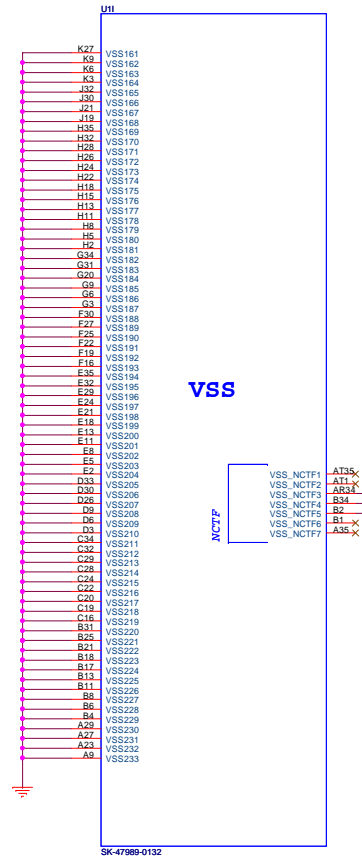
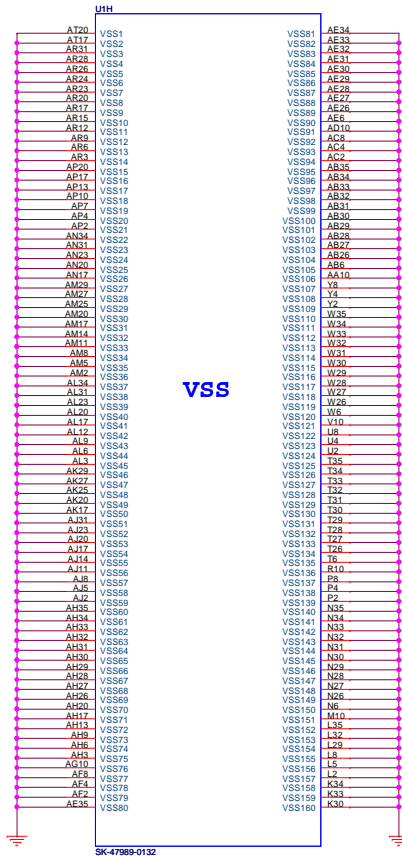
# ARRANDALE/CLARKSFIELD PROCESSOR (POWER)

Processor Core Power

Processor UNCore Power

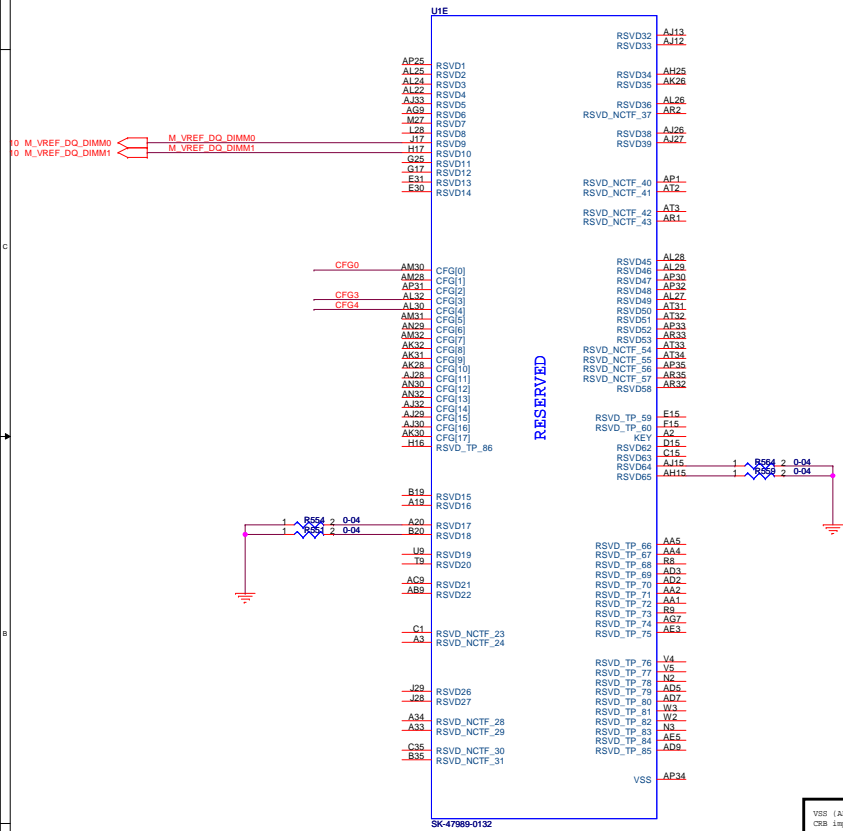


# AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

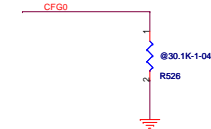




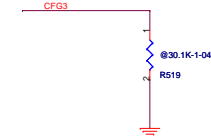
# AUBURNDALE/CLARKSFIELD PROCESSOR (RESERVED)



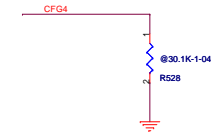
PCI-Express Configuration Select	
CFG0	1 : Single PEG 0 : Bifurcation enabled

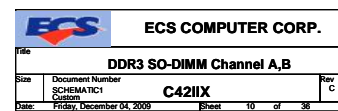


CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 : Normal Operation 0 : Lane Numbers Reversed



CFG4 - Display port presence	
CFG4	1 : Display , No physical display port attached to Embedded display port 0 : Enabled , An external display port device is connected to the Embedded display port

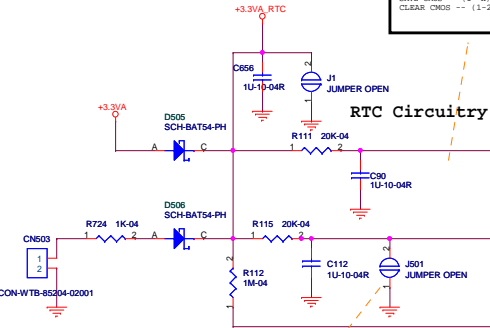




# IBEXPEAK - M (HDA,JTAG,SATA)

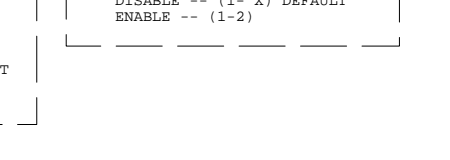
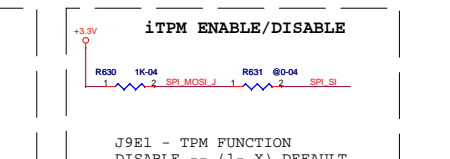
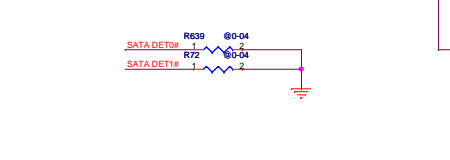
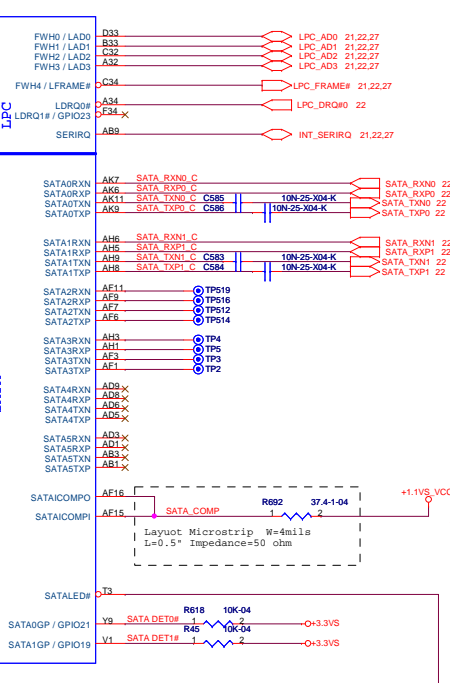
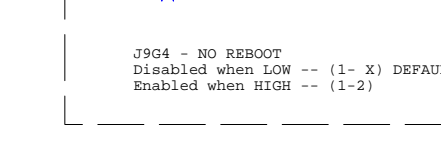
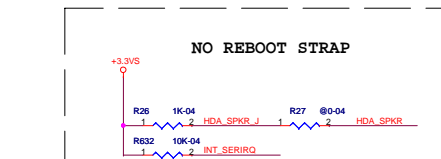
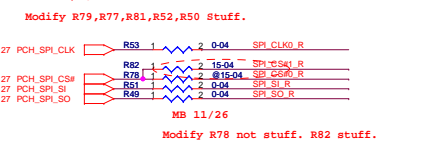
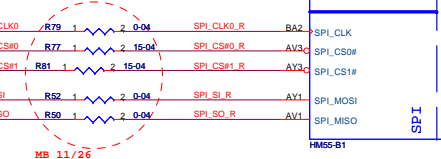
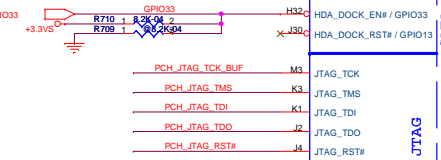
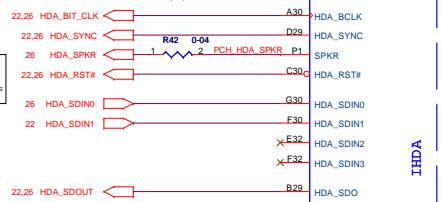
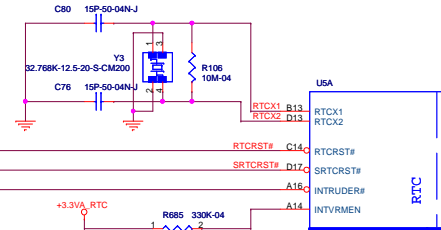
J5P2 - CMOS SETTING  
SAVE CMOS -- (1- X) DEFAULT  
CLEAR CMOS -- (1-2)

## RTC Circuitry

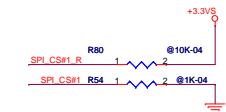
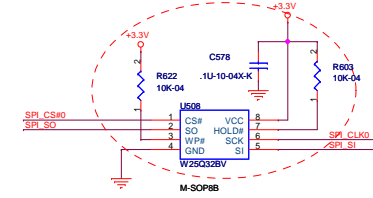


J5P1 - TPM SETTING  
SAVE ME PC REGISTER -- (1- X) DEFAULT  
CLEAR ME PC REGISTER -- (1-2)

INTVRMEN- Integrated SUS  
1.1V VBM Enable  
High - Enable Internal VBM

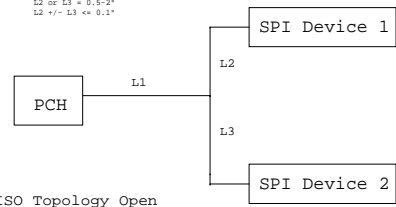


MB 11/26  
Modify U508,R622,c578,r603 stuff.

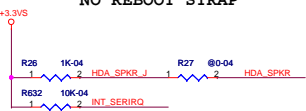


## Layout Topology for SPI CLK and MOSI

L1 = 1-5"  
L2 or L3 = 0.5-2"  
L2 +/- L3 <= 0.1"

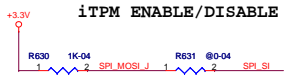


## NO REBOOT STRAP



J9G4 - NO REBOOT  
Disabled when LOW -- (1- X) DEFAULT  
Enabled when HIGH -- (1-2)

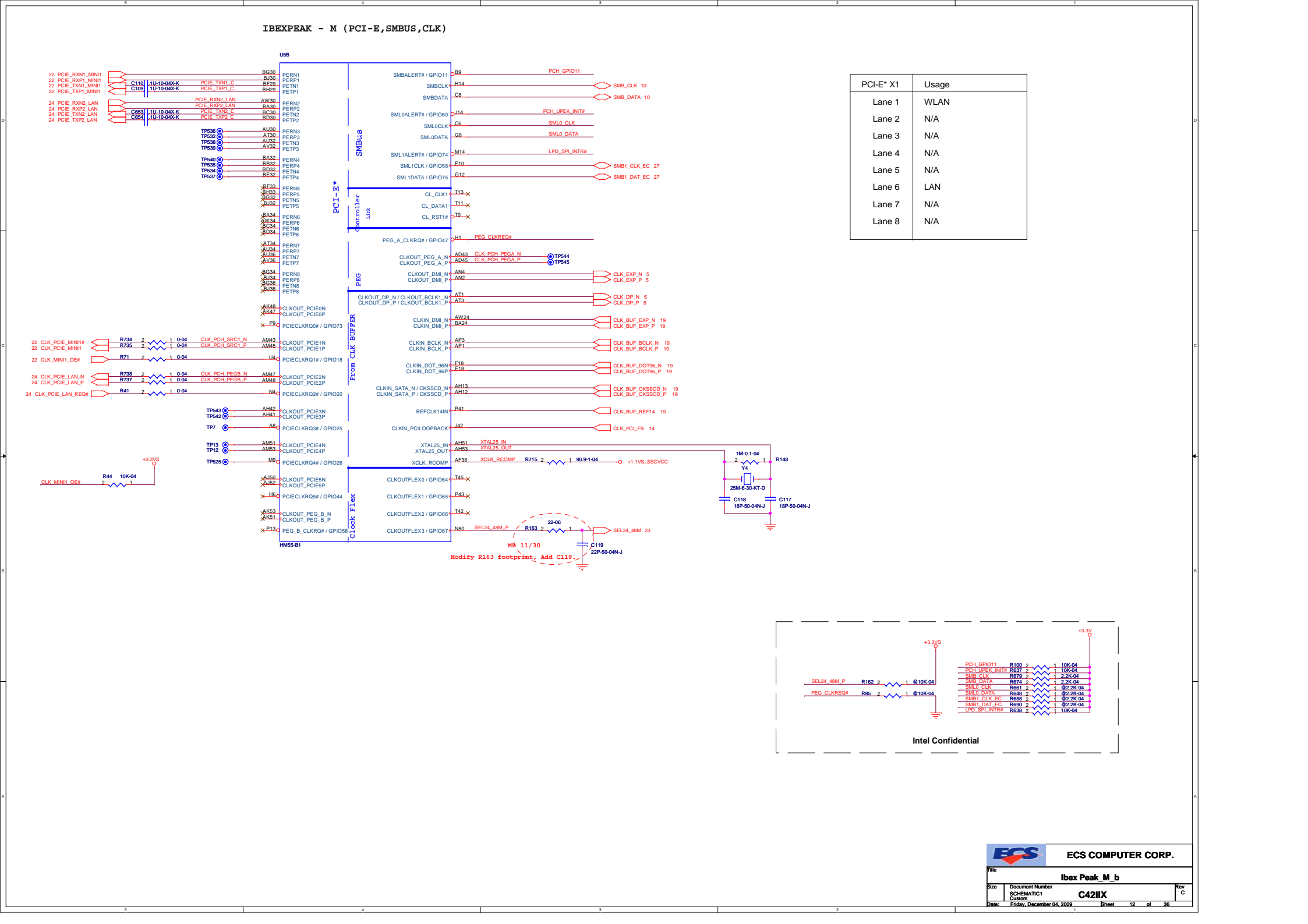
## iTPM ENABLE/DISABLE



J9E1 - TPM FUNCTION  
DISABLE -- (1- X) DEFAULT  
ENABLE -- (1-2)

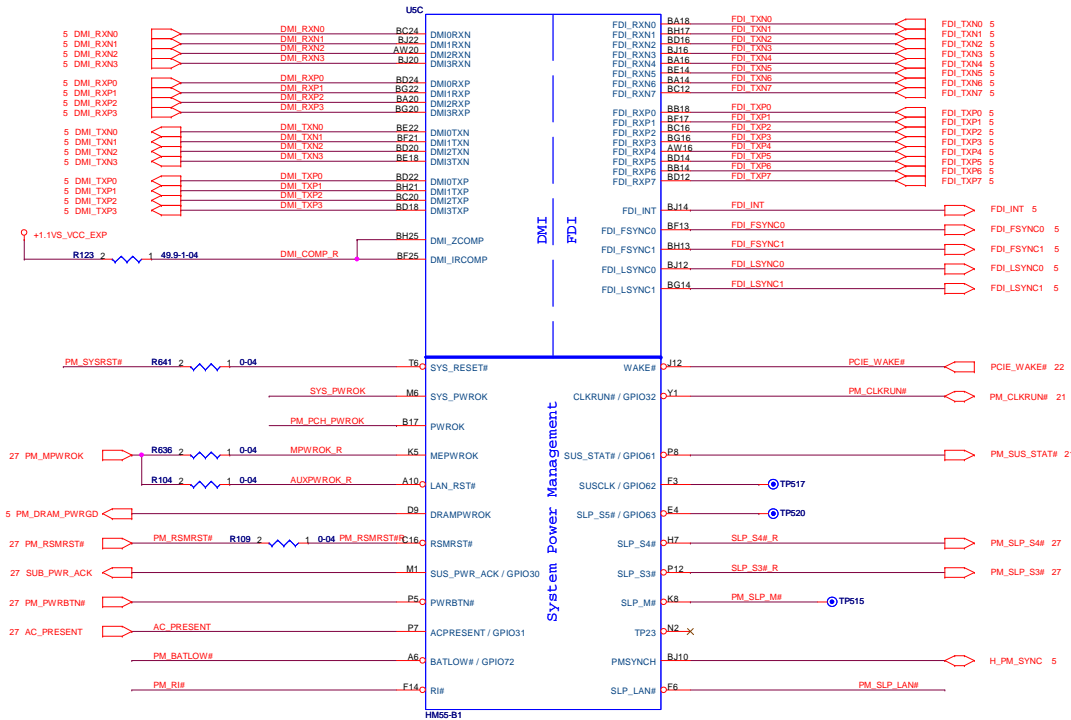
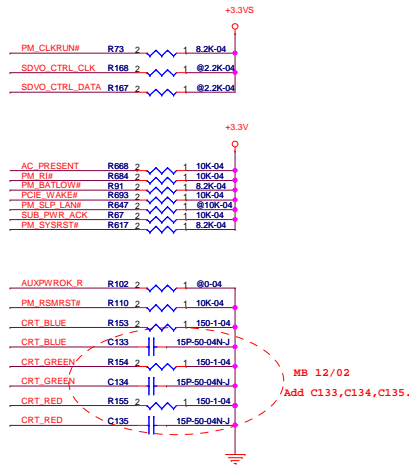
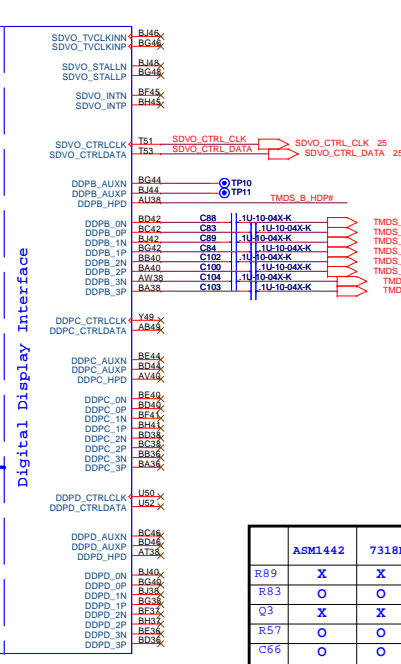
ECS COMPUTER CORP.

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Document Number  
C42IIX  
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Friday, December 04, 2009  
Sheet 11 of 38

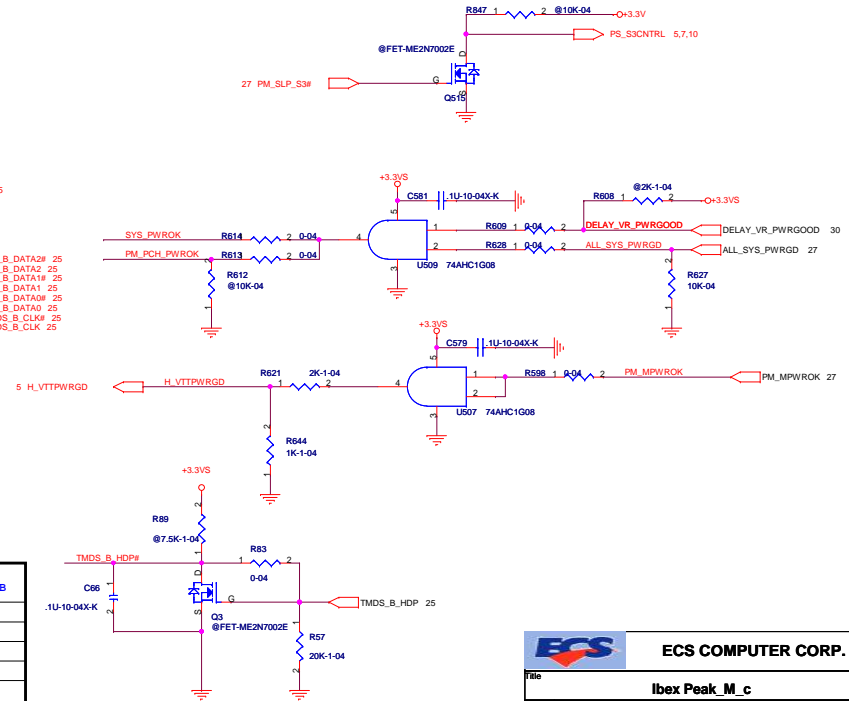


Common Motherboard Guidelines  
for FDI Disabling not  
followed, refer to Platorm Design Guide

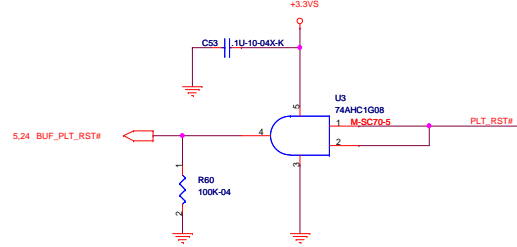
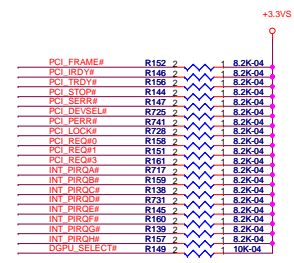
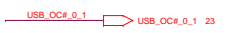
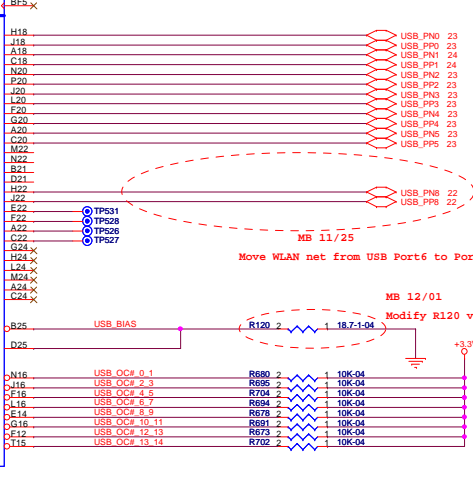
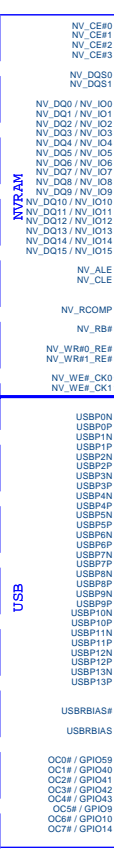
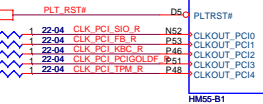
DDI Port B Detect		
SDVO_CTRL_DATA	1	Port B detected
	0	Port B not detected

[illegible]

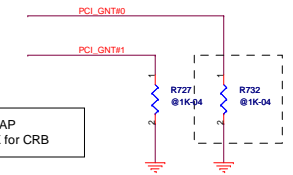
	ASM1442	7318B
R89	X	X
R83	O	O
Q3	X	X
R57	O	O
C66	O	O



	USE
X460	AD0
X34	AD1
C44	AD2
C38	AD3
X34	AD4
X46	AD5
D45	AD6
E36	AD7
H45	AD8
F40	AD9
C40	AD10
M45	AD11
F35	AD12
M40	AD13
M44	AD14
F38	AD15
K48	AD16
K48	AD17
K48	AD18
K48	AD19
K48	AD20
K46	AD21
K46	AD22
J52	AD23
K51	AD24
L34	AD25
F42	AD26
G46	AD27
F44	AD28
F44	AD29
F44	AD30
H38	AD31
J50	PB01#1 / PB01#1
H44	PB02#1 / PB02#1
G34	PB02#2 / PB02#2
G34	PB02#3 / PB02#3
G39	PIR0A#
H44	PIR0B#
H44	PIR0C#
H44	PIR0D#
F51	REQ0#
A46	REQ0#1 / GP050
H44	REQ0#2 / GP050
M55	REQ0#3 / GP054
F48	GN70#
X36	GN71# / GP051
H44	GN72# / GP051
H44	GN73# / GP055
B41	PIR0E# / GP012
K51	PIR0E# / GP012
K51	PIR0G# / GP012
K51	PIR0H# / GP012
K6	PIR5T#
E44	SER#
F44	PER#
A42	PLOCK#
RD4	RDY#
F46	DEVSEL#
F46	FRAME#
D49	PLOCK#
D41	STOP#
C46	TRDY#
X MC	PME#
D5	PLTRST#
N52	CLKOUT_PC0
N52	CLKOUT_PC1
N52	CLKOUT_PC2
N52	CLKOUT_PC3
N52	CLKOUT_PC4
DF P51	
P48	



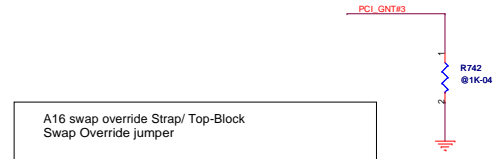
Buffer to reduce loading on PLT\_RST#



R? --BBS STRAP  
DEFAULT :1-X for CRB

BOOT BIOS STRAP		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

USBP0	Enchance USB USB_0
USBN0	
USBP1	USB BD USB_1
USBN1	
USBP2	USB BD USB_2
USBN2	
USBP3	Card Reader USB
USBN3	
USBP4	Web Camera USB
USBN4	
USBP5	Bluetooth USB
USBN5	
USBP6	
USBN6	
USBP7	
USBN7	WLAN USB
USBP8	
USBN8	
USBP9	
USBN9	
USBP10	
USBN10	
USBP11	
USBN11	



Danbury Technology  
Disabled when LOW  
Enabled when HIGH

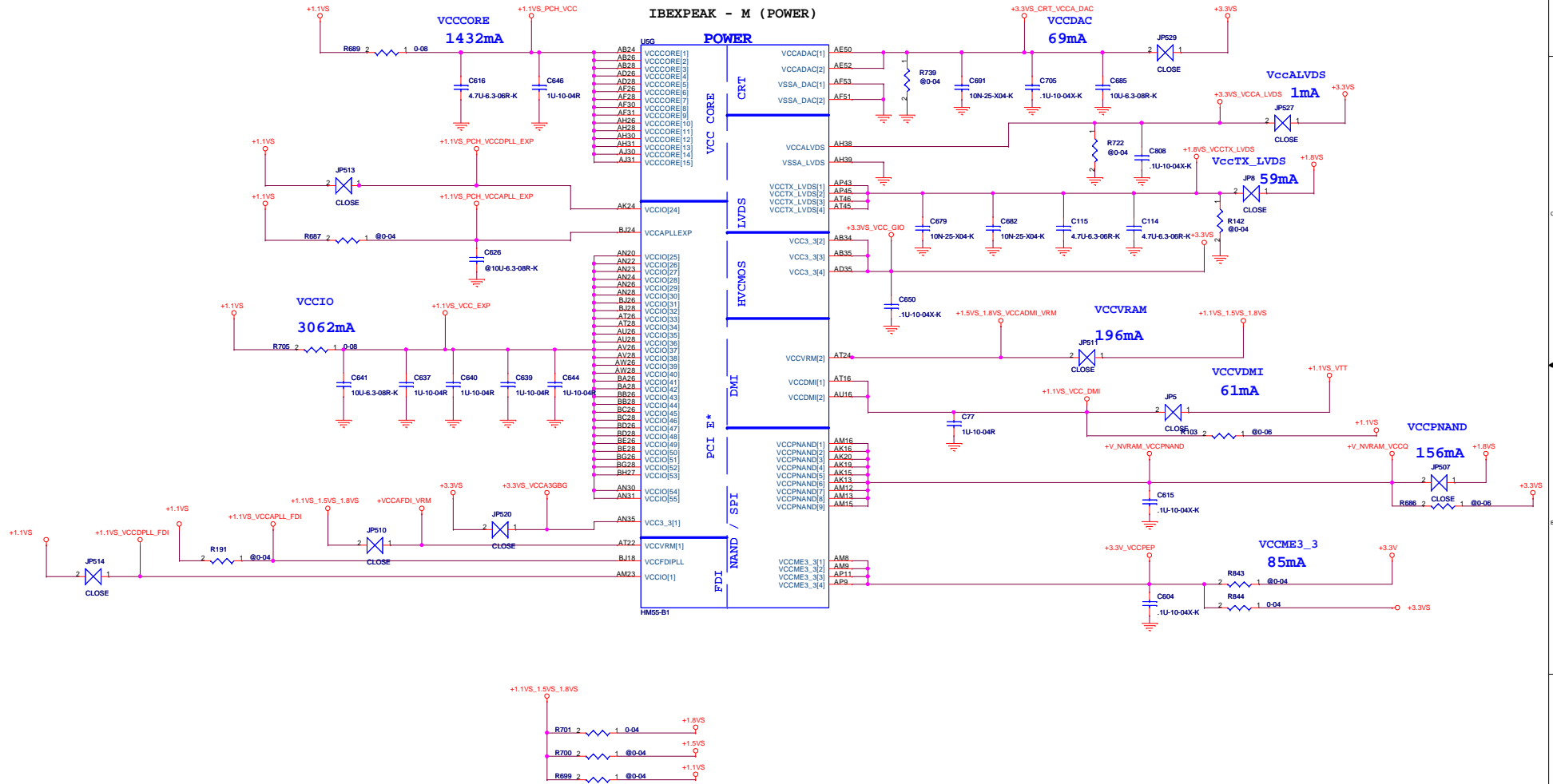
A16 swap override Strap/ Top-Block  
Swap Override jumper

PCI_GNT#3	LOW = A16 swap override/Top -Block Swap Override enabled High = Default
-----------	--

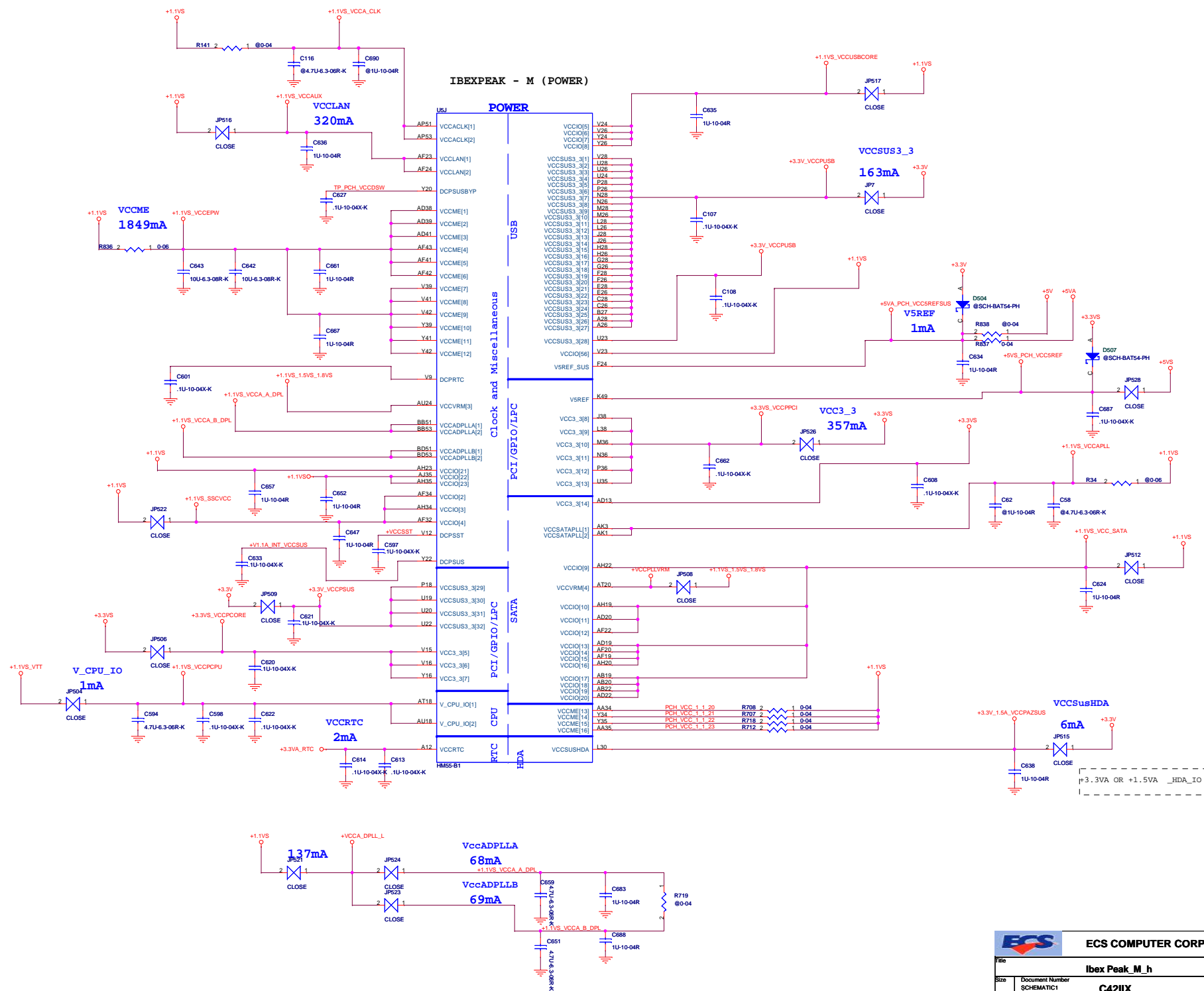


# IBEXPEAK - M (POWER)

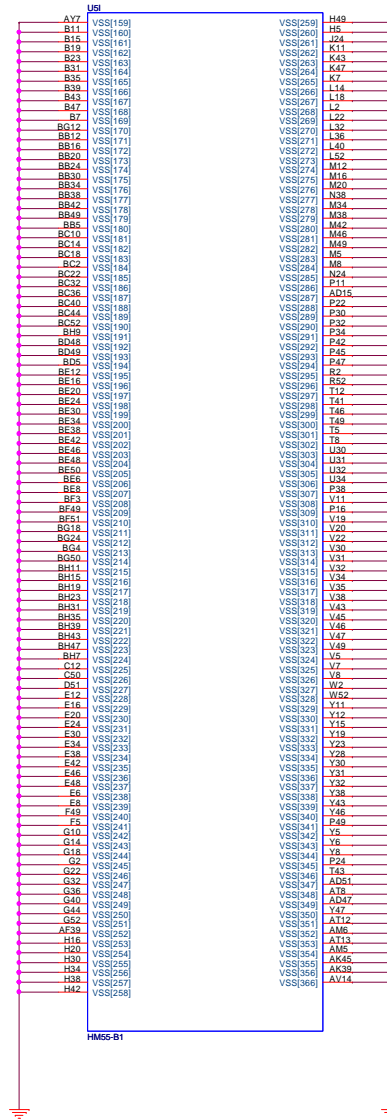
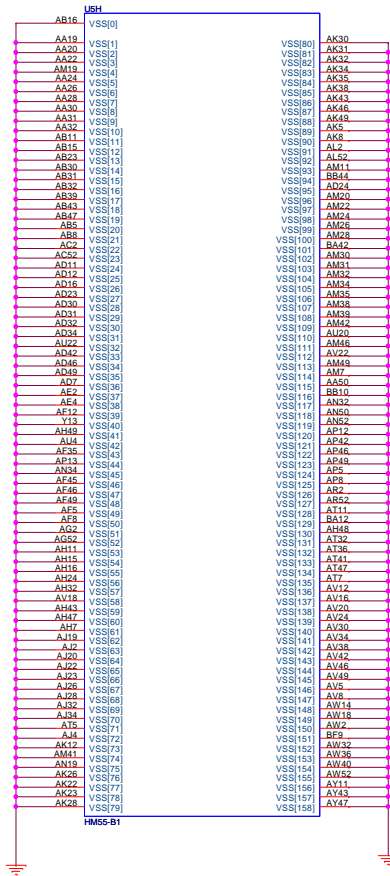
## POWER



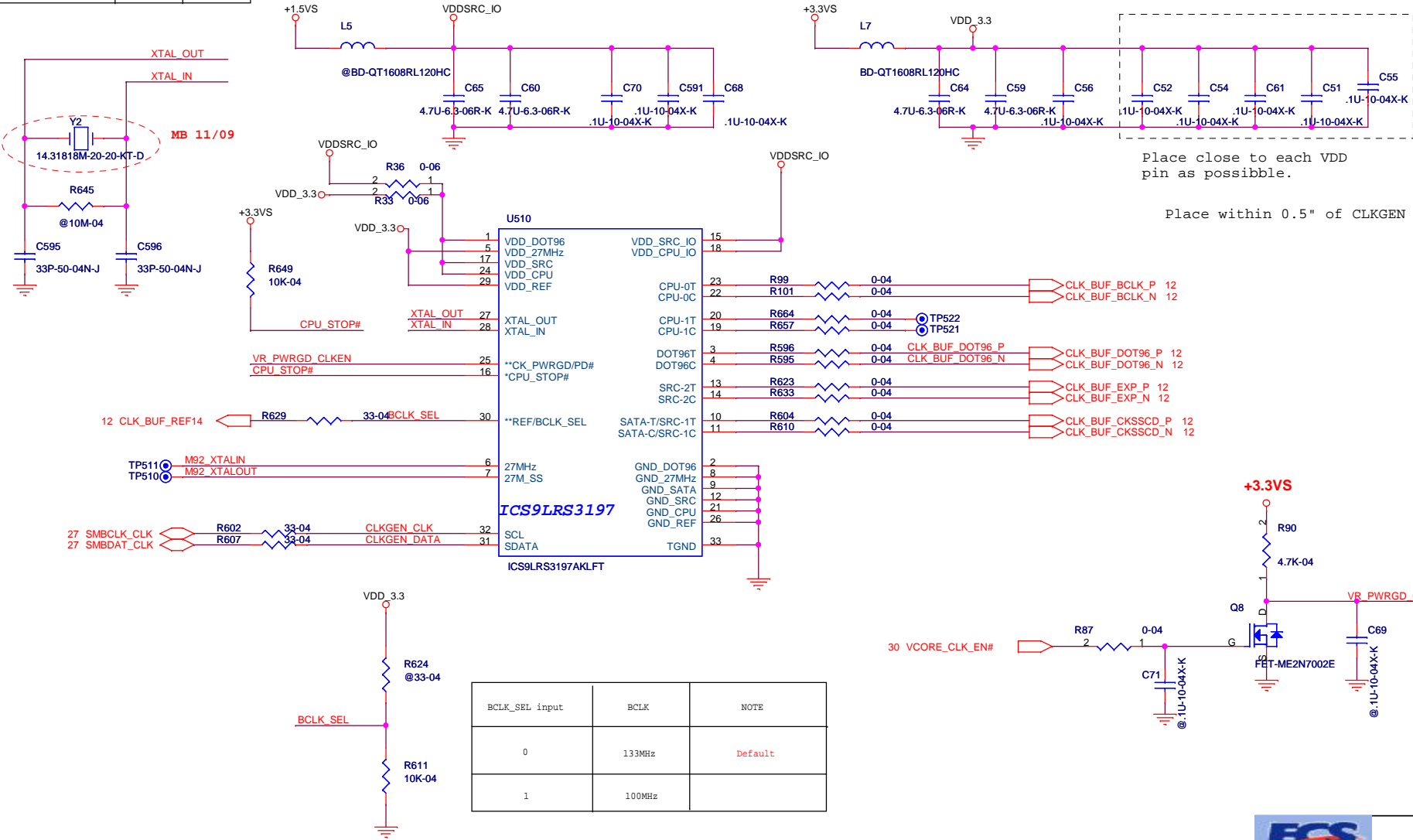





# IBEX PEAK-M (GND)



	L7	L5
ICS9LRS3197		
ICS9LVS3197		



CLK\_BUF\_REF14 12



**ECS COMPUTER CORP.**

Title

**CLOCK GEN (ICS9LRS3197)**

Size B

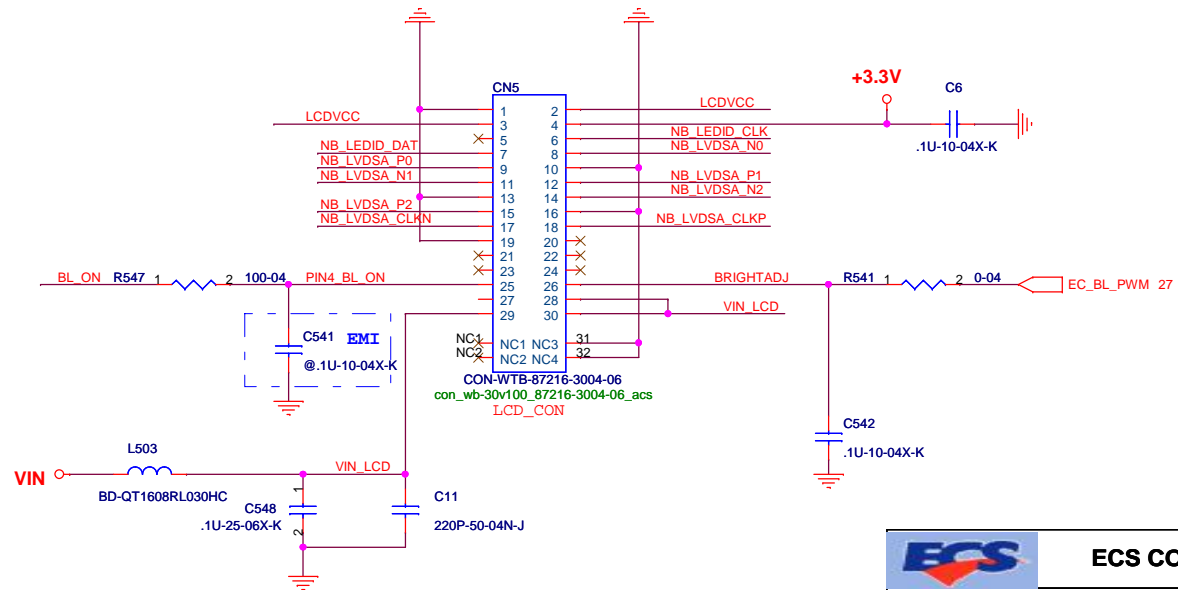
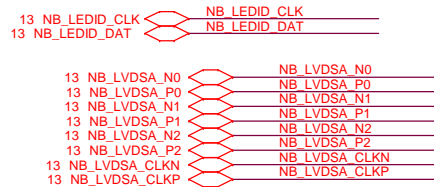
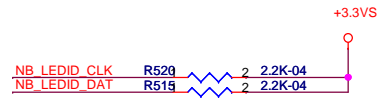
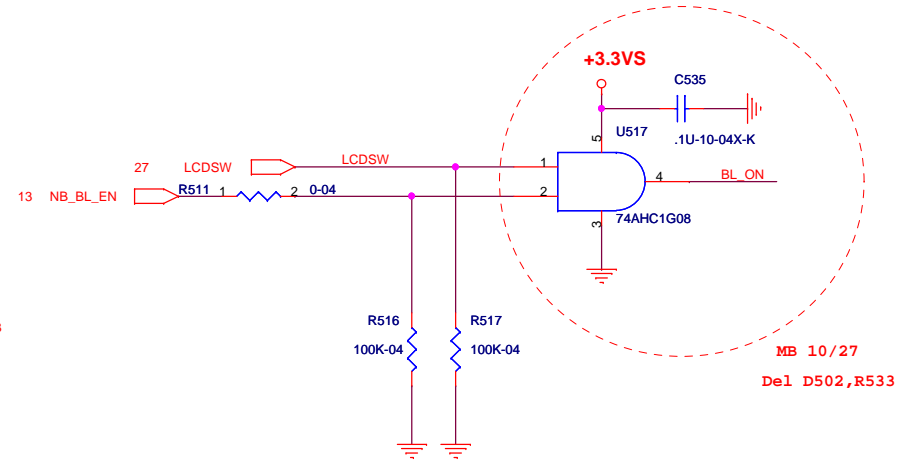
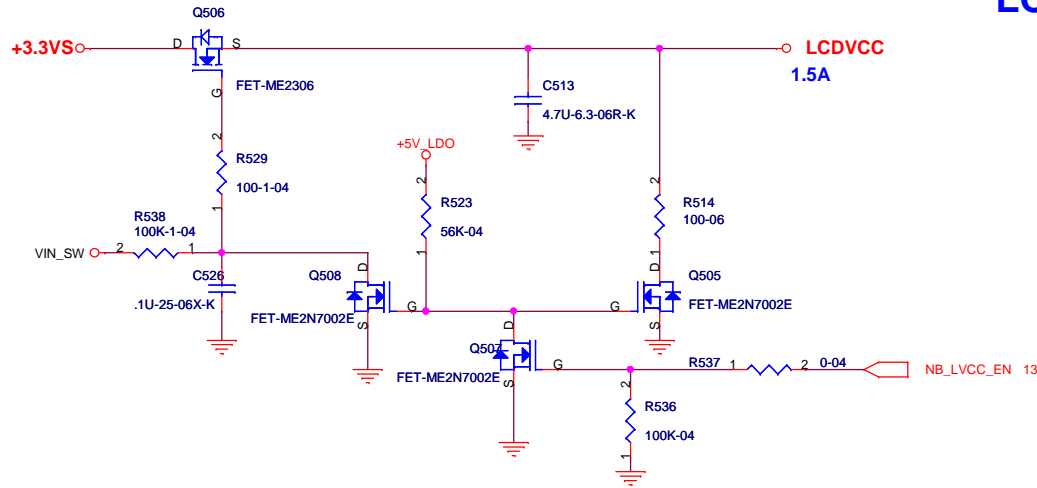
Document Number  
SCHEMATIC1

Rev C

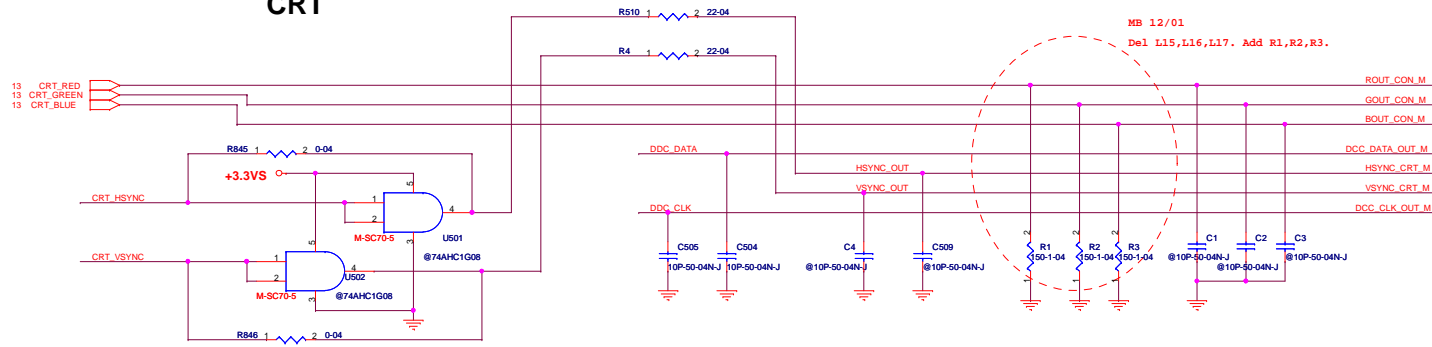
Date: Friday, December 04, 2009




Sheet 19 of 36

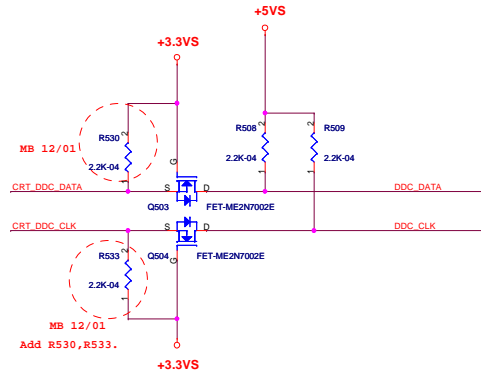
# LCD



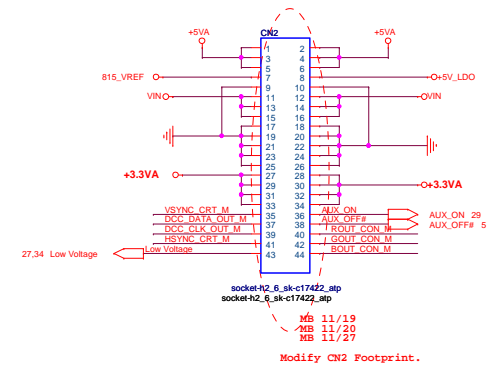
## CRT



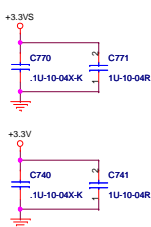
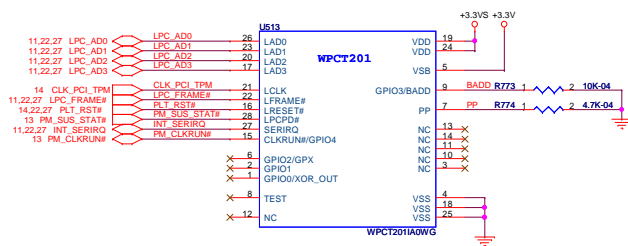
13	CRT_HSYNC		CRT_HSYNC
13	CRT_VSYNC		CRT_VSYNC
13,25	CRT_DDC_DATA		CRT_DDC_DATA
13,25	CRT_DDC_CLK		CRT_DDC_CLK



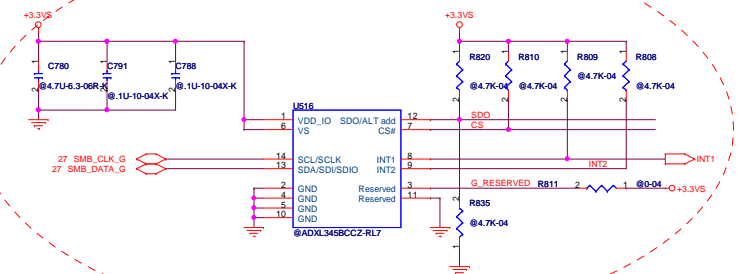
Connect to Power BD  
CRT/+3.3VA/+5VA Conn



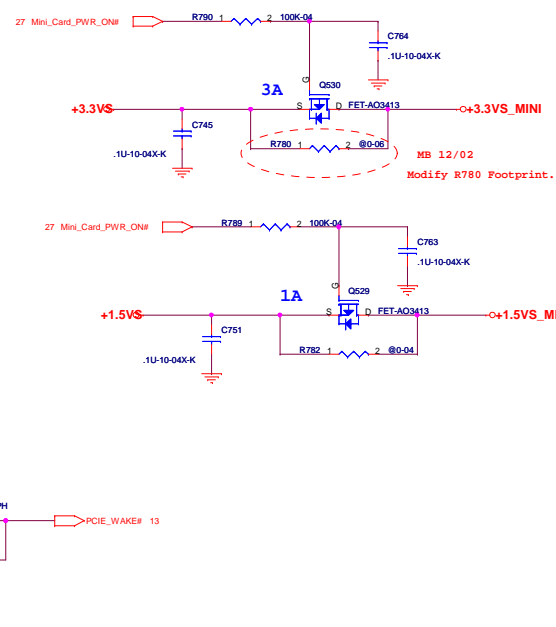
**TPM**



## G-Sensor



## WLAN\_CARD



**SATA HDD**

The diagram illustrates the electrical connections for a SATA Hard Disk Drive (HDD). It shows two main sections: a connector pinout on the left and a detailed power regulation circuit on the right.

### Connector Pinout

Signal / Component	Pin Number	Notes
SATA_TXP0	S1	C507   10N-25-X04-K
SATA_TXN0	S2	
C506	S3	
	S4	
SATA_RXND	S5	C508   10N-25-X04-K
	S6	
	S7	
	S8	
V_HDD1	P1	
	P2	
	P3	
	P4	
	P5	
	P6	
	P7	
	P8	
	P9	
	P10	
R178	P11	
	P12	
	P13	
	P14	
	P15 NC2	
GND1	NC1	
GND2	NC2	

### Power Regulation Circuit

This circuit converts a +5V input to a regulated 1.5A output for V\_HDD1.

- Input:** +5V
- Inductor:** L1 (60MIL)
- Capacitors:** C5 (input), C7 (output), C10 (output filter)
- IC:** BD-QT1608L0R0HC
- Output:** 1.5A at V\_HDD1

**Component Values:**

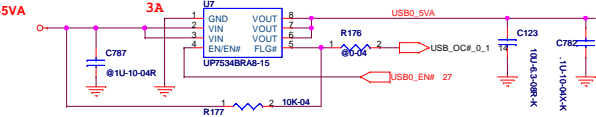
- L1: 60MIL
- C5: 4.7µF ±0.1K
- C7: 4.7µF ±0.1K
- C10: 1U10-04X-K

**Legend:**

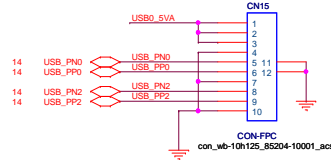
```
con_hdd_550v_c160bp-12205-_stp
con_hdd_550v_c160bp-12205-_stp
```

[illegible][illegible]

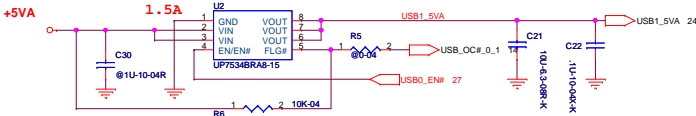
## USB0/USB2



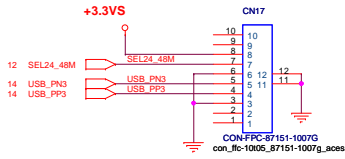
## Connect to USB BD USB CONN



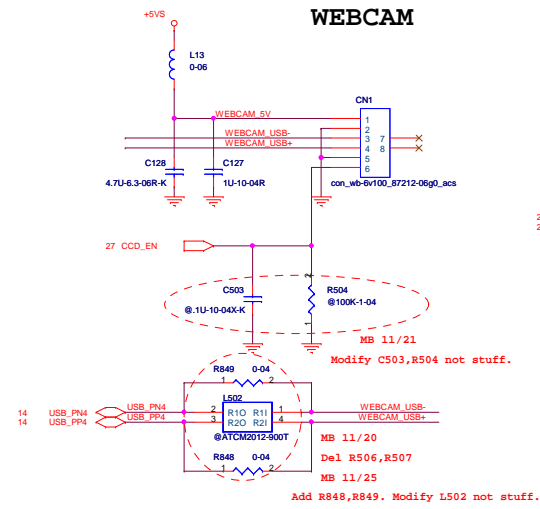
## USB1



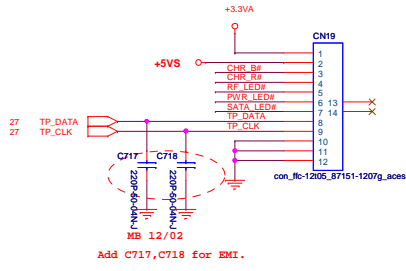
## Connect to Card Reader Card Reader Conn



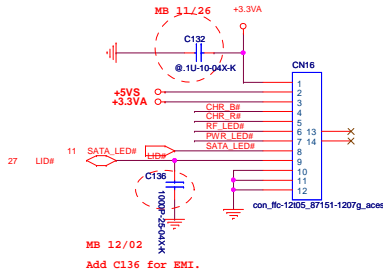
## WEBCAM



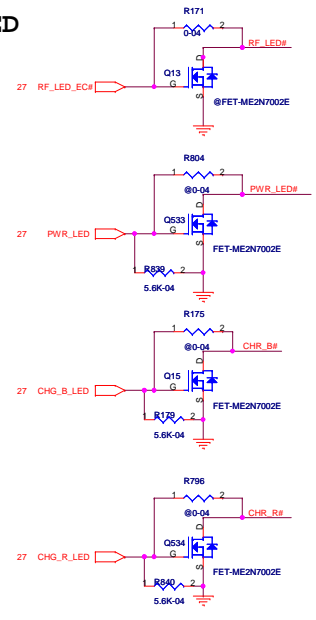
## Connect to TP+LED BD TP+LED Conn



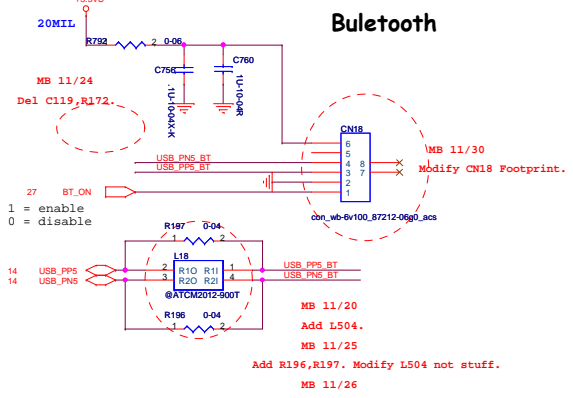
## Connect to LED/LID BD LED/LID CONN

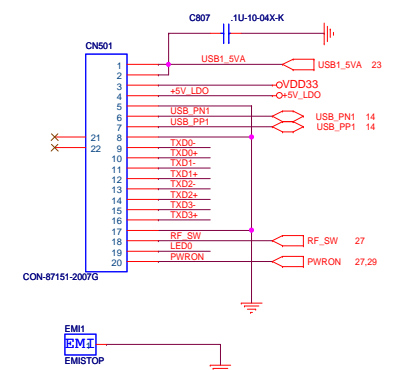
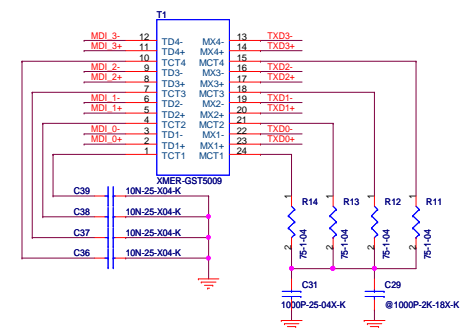
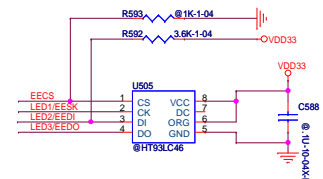
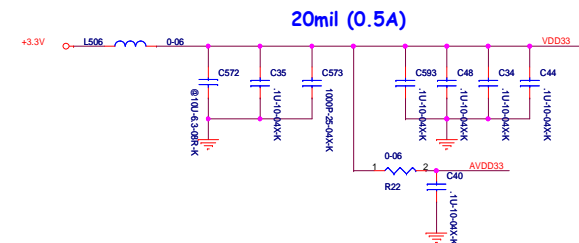


## LED



## Buletooth

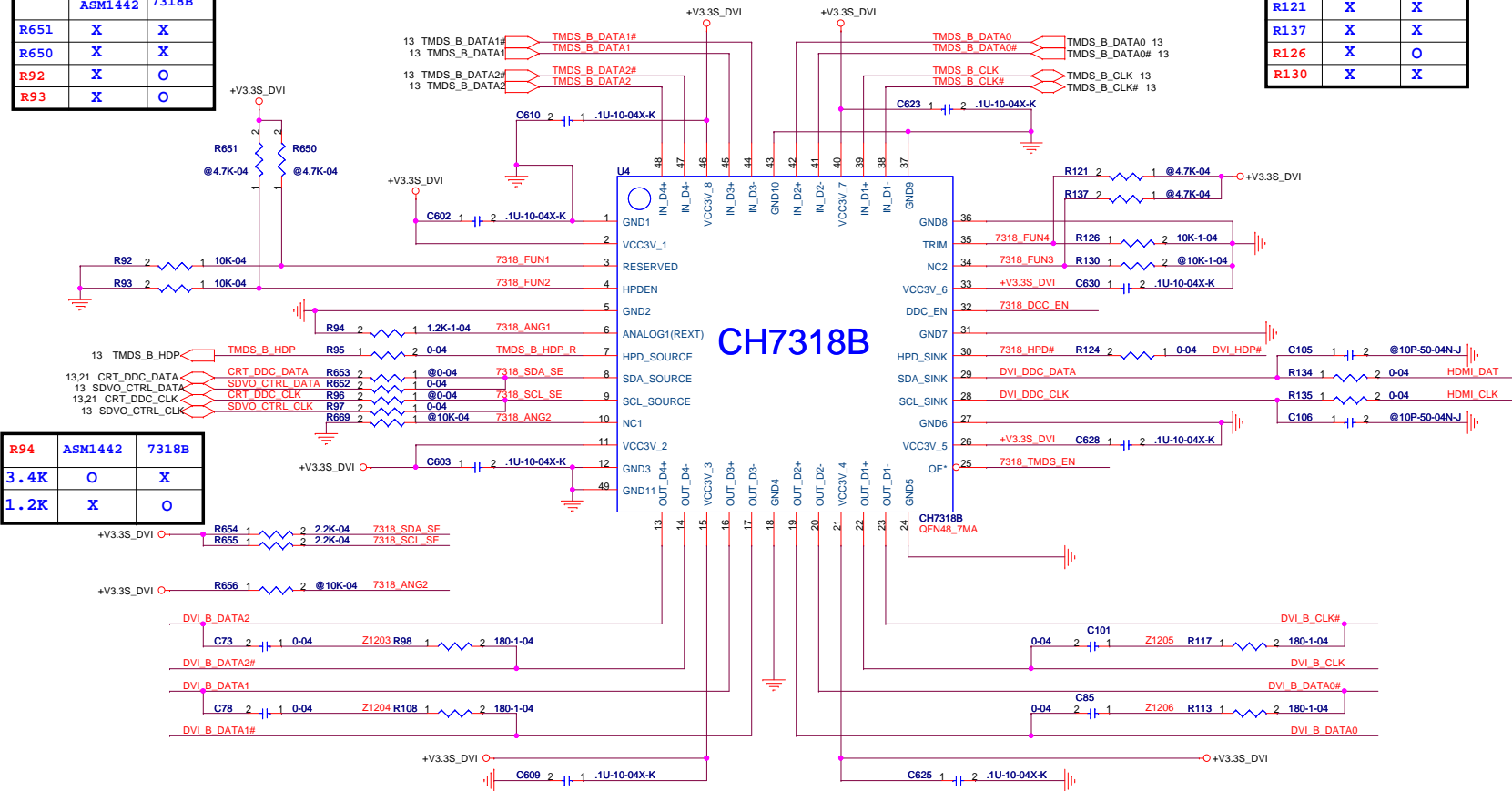






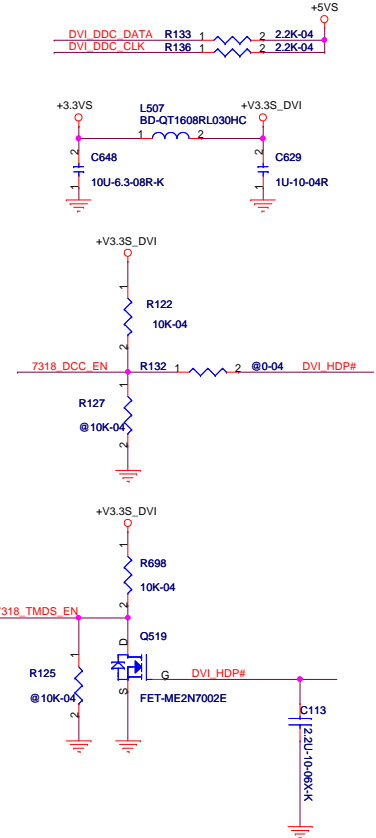
# DVI SHIFTER

	ASM1442	7318B
R651	X	X
R650	X	X
R92	X	O
R93	X	O



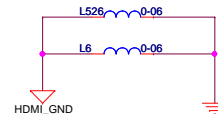
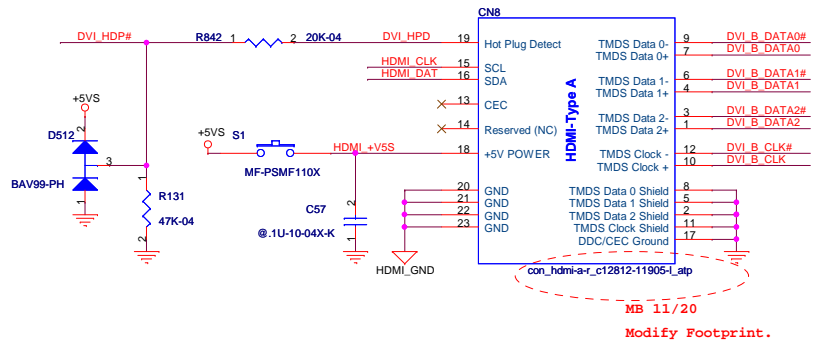
R94	ASM1442	7318B
3.4K	O	X
1.2K	X	O

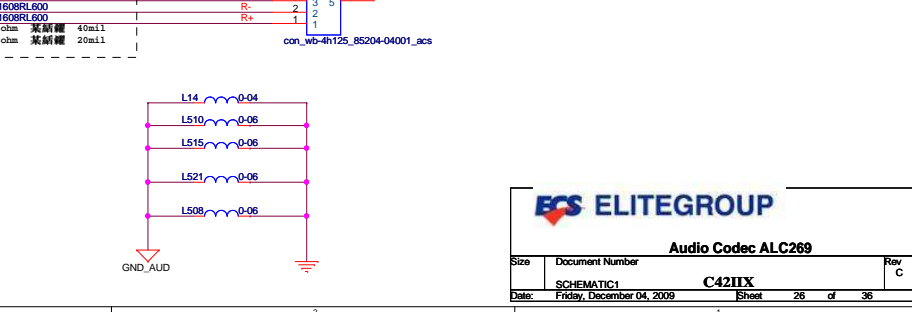
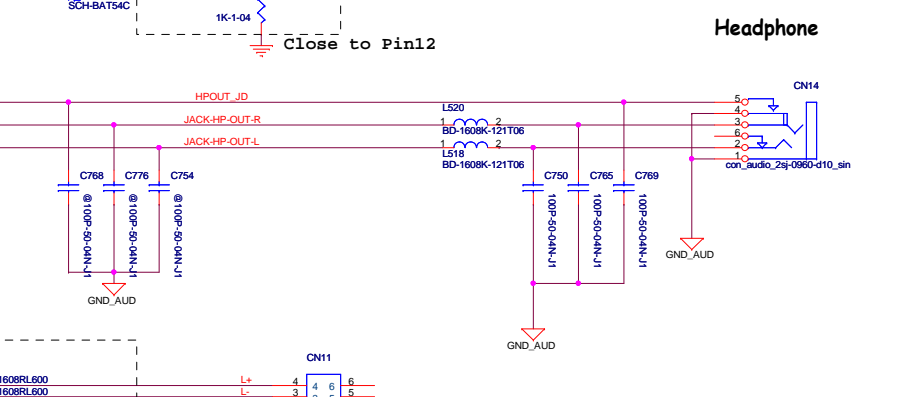
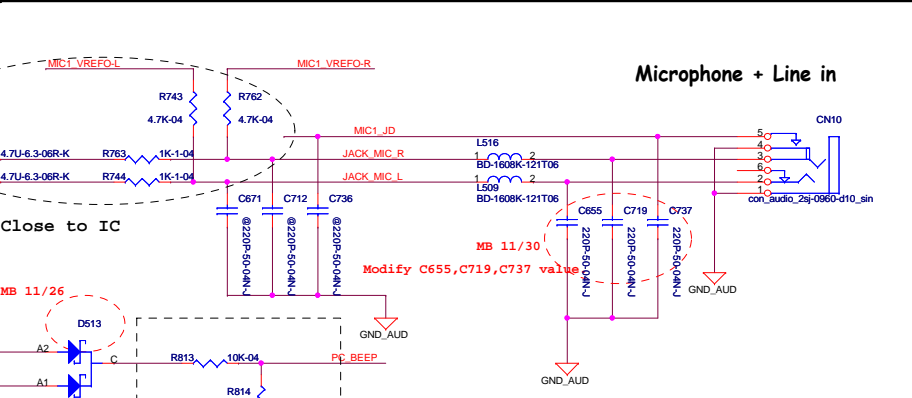
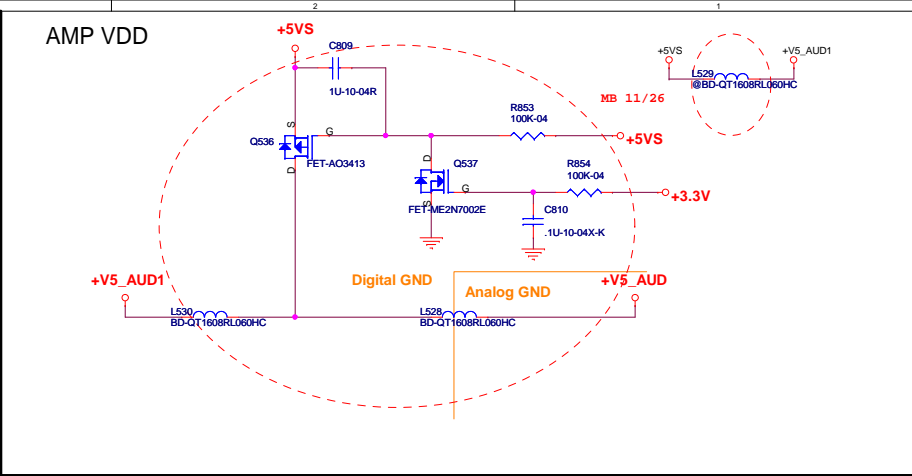
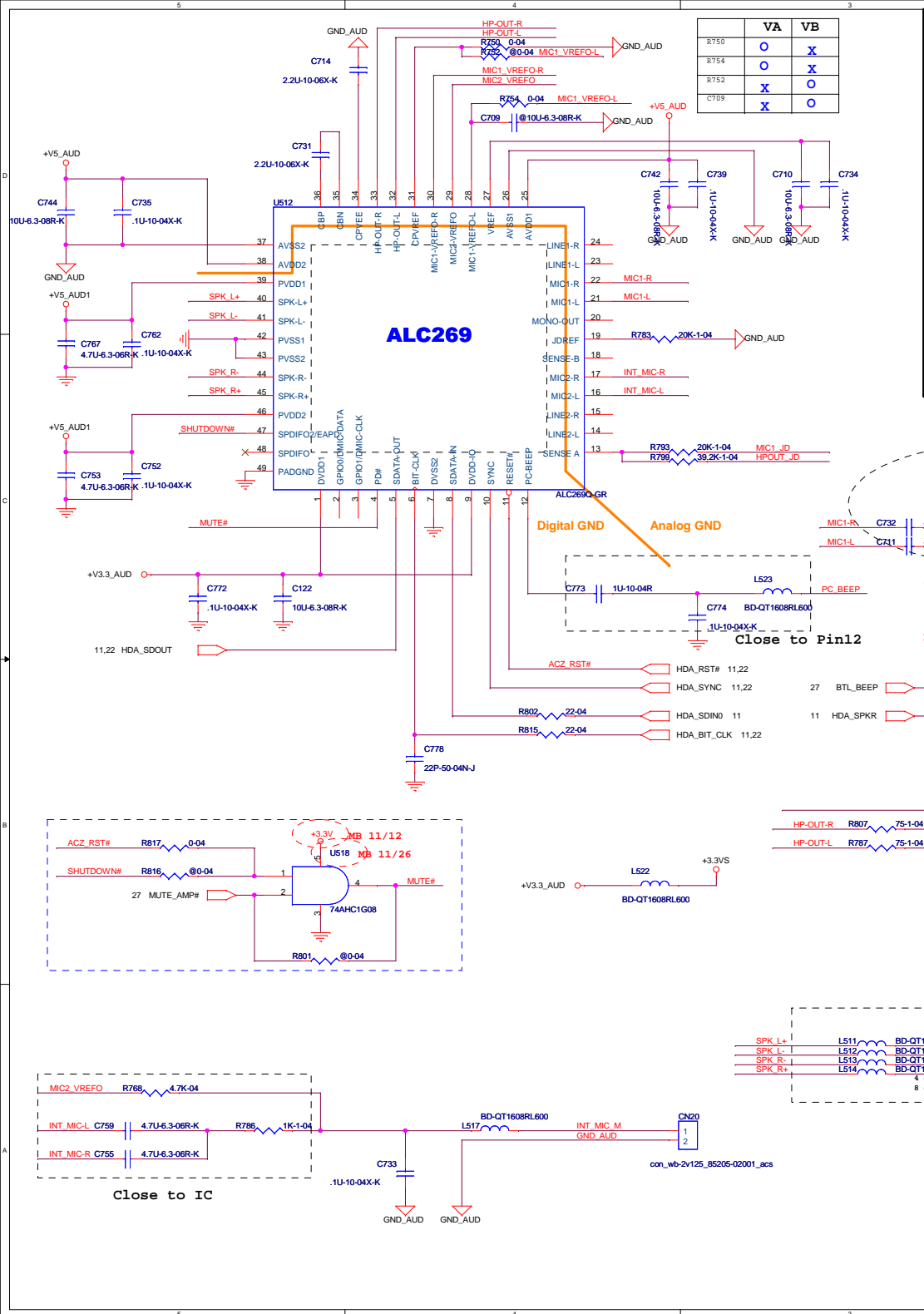
	ASM1442	7318B
R121	X	X
R137	X	X
R126	X	O
R130	X	X

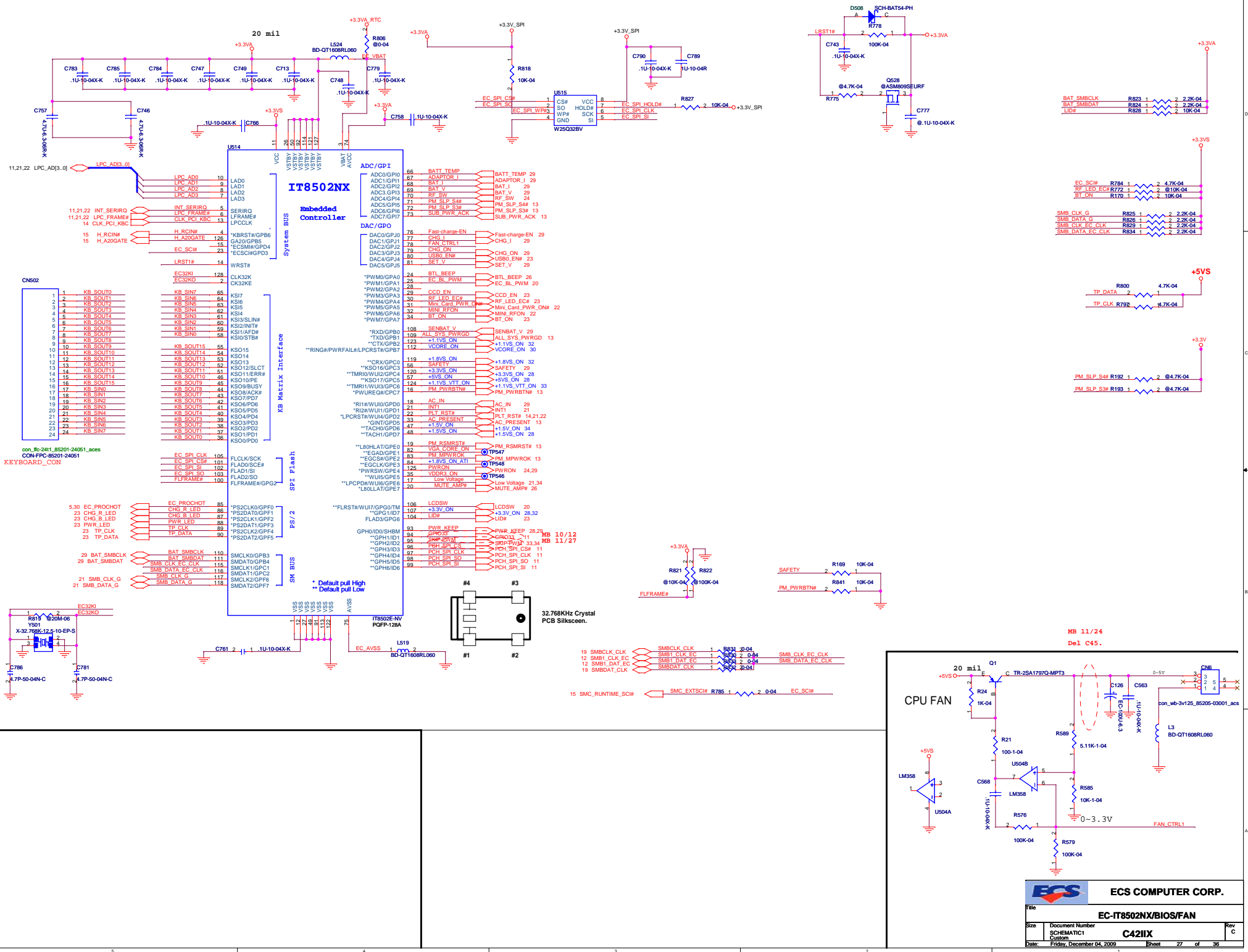


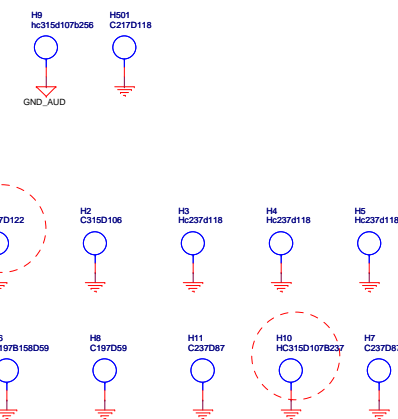
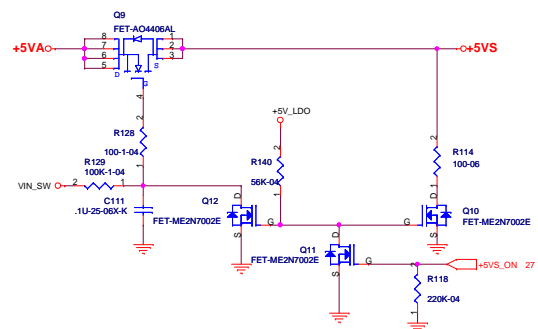
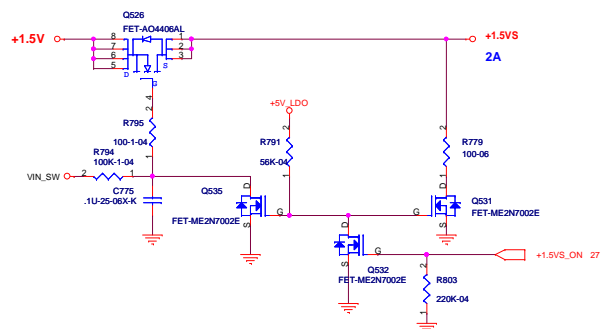
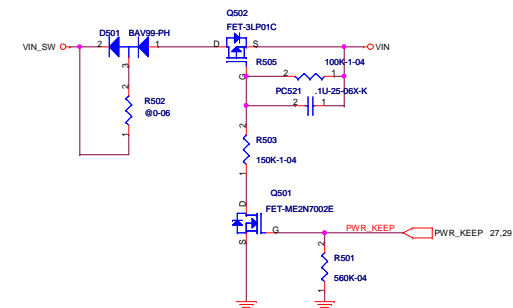
	ASM1442	7318B
R117	X	O
C101	X	O
R113	X	O
C85	X	O
R108	X	O
C78	X	O
R98	X	O
C73	X	O

## HDMI Conn.

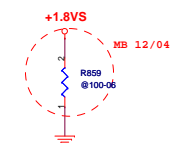
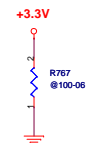
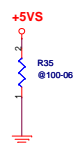
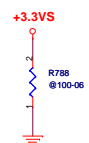
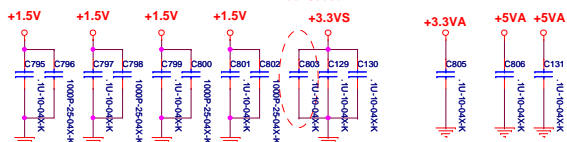




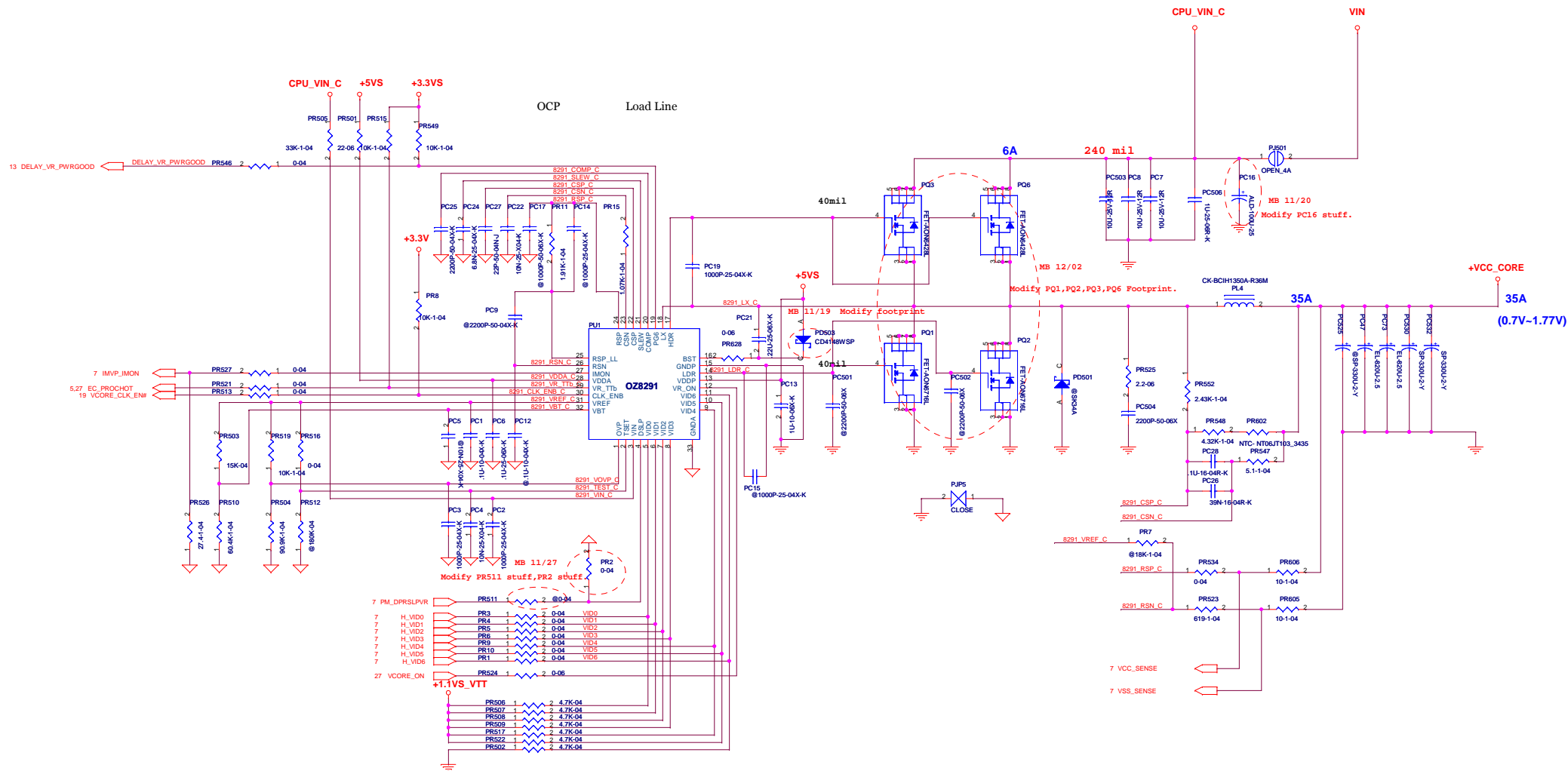




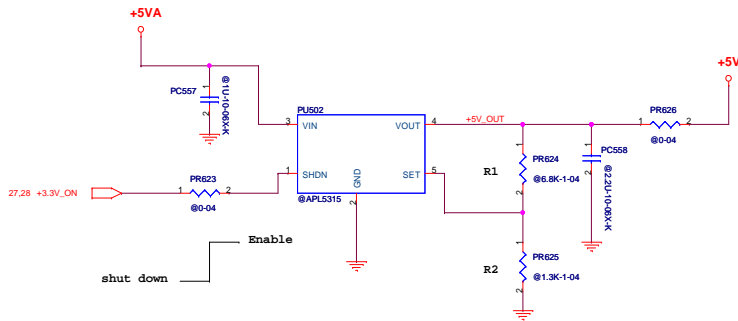
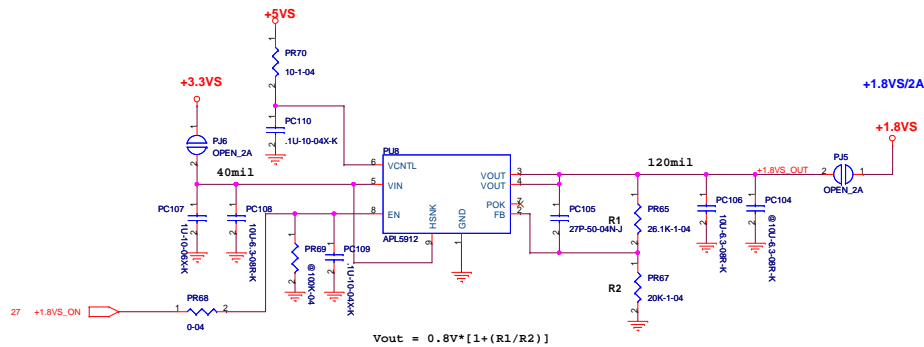
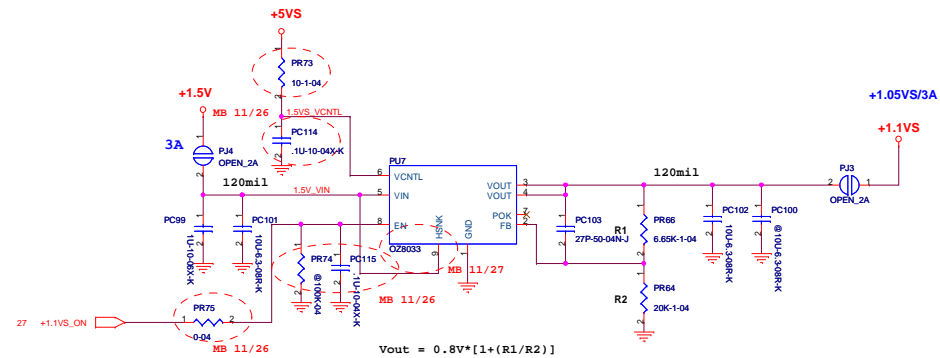
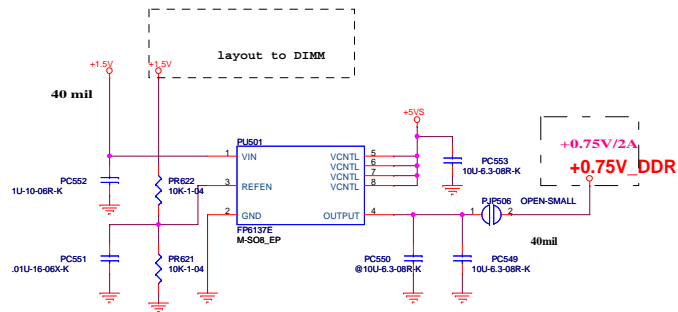
MB 12/02  
Add C803.









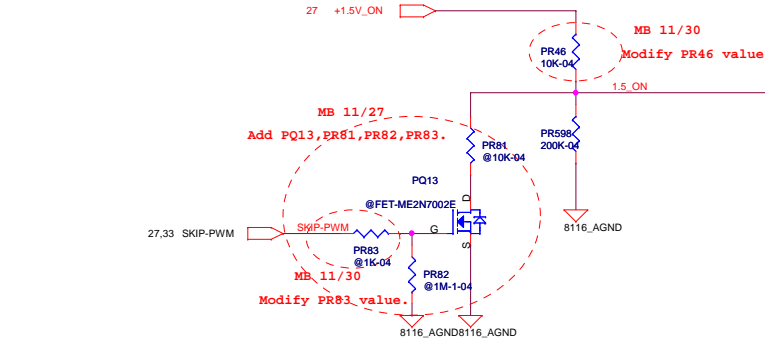






EC L=1.509V  
EC H=1.432V

21,27 Low Voltage



+1.5 CSN  
+1.5 CSP  
+1.5 LX

+1.5 HDR

+5V

+1.5 SET  
+1.5 REF

2.75V

1.5\_VIN

1.5\_ON

1.5\_VIN

1.5\_ON

1.5\_VIN

1.5\_ON

1.5\_VIN

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1.5\_ON

1.5\_VIN

1.5\_ON

+1.5 CSN  
+1.5 CSP  
+1.5 LX

+1.5 HDR

+5V

+1.5 SET  
+1.5 REF

2.75V

1.5\_VIN

1.5\_ON

1.5\_VIN

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1.5\_VIN

1.5\_ON

+1.5 CSN  
+1.5 CSP  
+1.5 LX

+1.5 HDR

+5V

+1.5 SET  
+1.5 REF

2.75V

1.5\_VIN

1.5\_ON

1.5\_VIN

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1.5\_ON

+1.5 CSN  
+1.5 CSP  
+1.5 LX

+1.5 HDR

+5V

+1.5 SET  
+1.5 REF

2.75V

1.5\_VIN

1.5\_ON

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1.5\_ON

+1.5 CSN  
+1.5 CSP  
+1.5 LX

+1.5 HDR

+5V

+1.5 SET  
+1.5 REF

2.75V

1.5\_VIN

1.5\_ON

1.5\_VIN

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1.5\_ON

+1.5 CSN  
+1.5 CSP  
+1.5 LX

+1.5 HDR

+5V

+1.5 SET  
+1.5 REF

2.75V

1.5\_VIN

1.5\_ON

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1.5\_ON

+1.5 CSN  
+1.5 CSP  
+1.5 LX

+1.5 HDR

+5V

+1.5 SET  
+1.5 REF

2.75V

1.5\_VIN

1.5\_ON

1.5\_VIN

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1.5\_VIN

1.5\_ON

+1.5 CSN  
+1.5 CSP  
+1.5 LX

+1.5 HDR

+5V

+1.5 SET  
+1.5 REF

2.75V

1.5\_VIN

1.5\_ON

1.5\_VIN

1.5\_ON

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1.5\_ON

1.5\_VIN

1.5\_ON

1.5\_VIN

1.5\_ON

+1.5 CSN  
+1.5 CSP  
+1.5 LX

+1.5 HDR

+5V

+1.5 SET  
+1.5 REF

2.75V

1.5\_VIN

1.5\_ON

1.5\_VIN

1.5\_ON

1.5\_VIN

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1.5\_ON

1.5\_VIN

1.5\_ON

+1.5 CSN  
+1.5 CSP  
+1.5 LX

+1.5 HDR

+5V

+1.5 SET  
+1.5 REF

2.75V

1.5\_VIN

1.5\_ON

1.5\_VIN

1.5\_ON

1.5\_VIN

1.5\_ON

1.5\_VIN

1.5\_ON

1.5\_VIN

1.5\_ON

1.5\_VIN

1.5\_ON

1.5\_VIN

1.5\_ON

1.5\_VIN

1.5\_ON

1.5\_VIN

1.5\_ON

$$F = V_{out}(V_{in} - V_{out}) / (4.4 * V_{in}) = 226KHz$$

+1.5V/8A

1.5V

OCP 12A

I<sub>out</sub>=3.2A  
OCP=4.8A  
I=0.94V  
Ripple=4.7mV  
F=226kHz

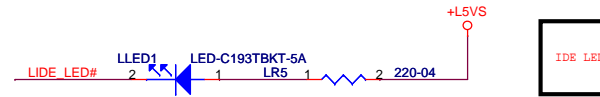
**ELITEGROUP**

+1.1VS\_VTT (OZ8138)

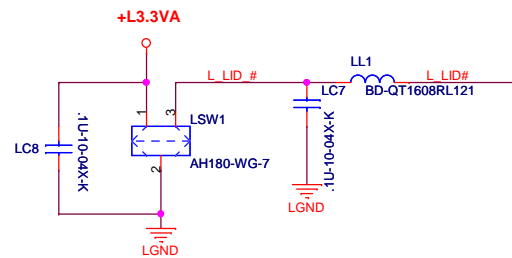
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	SCHEMATIC1	C
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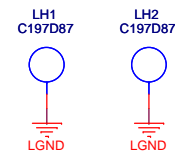
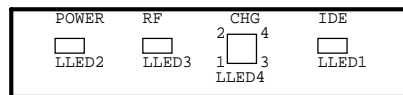
PCB2  
PCB  
35G4C4230-C0



**LID**



Color If	Sus/Wireless	Charger	
	Blue	Blue	Red
5mA	390_1	390_1	560_1
20mA	90.9	100	140



**ECS COMPUTER CORP.**

Title

**LED/LID BD**

Size

Document Number
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**C42II**

Date \_\_\_\_\_

Friday, December 04, 2009

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